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Analysis and Design of a Tapped Inductor Boost Converter for a High Voltage Gain Application

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Analysis and Design of a Tapped Inductor Boost Converter for a High Voltage Gain Application

by

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Abstract

Analysis and Design of a Tapped Inductor Boost Converter for a High Voltage Gain Application

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The University of Texas at Austin, 2021

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High voltage gain power converters are required in many applications, especially in integration of solar energy with the grid. This thesis provides an effective solution for the same in the form of a Tapped Inductor Boost converter. This work provides a complete guide to the design process that can be followed for a high performance high voltage gain converter. High frequency (HF) operation of the converter is proposed to maximize the potential of the topology. HF operation includes some challenges and the solutions for the same are provided. A 20-400V, 400W prototype is designed and developed which serves as a platform to test low leakage transformer and to highlight the performance of the converter

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Chapter 1: Introduction

Many applications require a high step-up dc-dc converter. These applications include fuel cells, photovoltaic systems, data centers, and uninterrupted power supplies [1]. Considering the example of a photovoltaic system, a PV panel generates a DC voltage in the range of 12-24volts. To integrate a PV plant with the grid, this output is very low and needs a very high step-up. One possibility is to add the panels in series to boost the voltage to the desired value (300-400V). This is always avoided, as failure to one PV panel would mean total failure of the plant. Hence, a high conversion ratio dc-dc converter is an essential to integrate a PV plant with the grid.

The Tapped Inductor Boost converter is a DC-DC converter that can be a possible solution for a high DC voltage step-up requirements, where no isolation is required. The advantages include low switch stresses, high reliability and low duty operation. This work discusses these advantages and some limitations (also provide effective solution to overcome them). The complete design strategy, its implementation, and the development of a prototype to showcase the performance of this converter are presented in this work.

FINDING A CONVERTER FOR HIGH VOLTAGE GAIN APPLICATION

The most basic converter used to provide a voltage gain is a traditional boost converter. In case of a high voltage gain requirement, using the conventional boost converter would mean it would have to be operated at a very high duty cycle. This would translate into very high resistive losses due to high rms currents for the same the power requirement. Also, the high voltage stress on the switches is a disadvantage. This is because a switch with higher breakdown voltage is required meaning poorer FOM, higher stored

energy switching losses, and more expensive. These limitations makes the boost converter an impractical solution for high voltage gain applications.

To overcome the limitations of operation at an extreme duty cycle, cascaded dc/dc converters have been proposed [2][3]. Even though this strategy may seem viable, critical disadvantages arise from cascade structures. They generally include numerous components, complex control, and high switch stresses [4].

Switched capacitor converters can also be used to obtain a high voltage gain [5][6]. To obtain a very high voltage conversion ratio, a cascade of converters is needed, again resulting in numerous components and complex control. High power application would also mean the switched capacitors would have high current spikes, causing lower efficiency.

Converters employing Coupled Inductors (also called as Tapped Inductor) offer a simple yet effective solution to get the desired high voltage gain without compromising on efficiency, reliability, and performance. The simplest coupled inductor topology is the Tapped Inductor Boost Converter [7][8].

A Tapped Inductor Boost converter is obtained by a small topological modification to a boost converter. Using this topology basically means escaping very high-duty cycle operation for similar voltage gain. This would mean efficient power conversion. Also, the switch stresses are lower. This topology has fewer components (higher reliability), is easy to implement, and can be designed for performance on par with other commonly used converter topologies.

BASICS OF THE TAPPED INDUCTOR BOOST CONVERTER

The Tapped Inductor is the magic component of this converter. It allows for the converter to operate at a much lower duty cycle as compared to a conventional boost to

obtain the same voltage gain. The basic structure of the Tapped Inductor converter is shown in Figure 1. It is not much different than a conventional boost converter. The important difference is that the inductor is tapped, and hence provides a 1: N turns ratio. This turns ratio provides an additional voltage boost at the output and thereby allows operation at much lower duty cycles. The lower duty cycle significantly diminishes resistive losses since rms currents decreases significantly for same average current processed, even for higher voltage step-up requirements. Less resistive loss translates into higher converter efficiency and makes it practical to implement such a converter. Moreover, the switch no longer needs to support the high output voltage during the turn off operation. Hence, a switch with a better Figure of Merit (FOM) can be implemented, which provides another opportunity to improve converter performance.

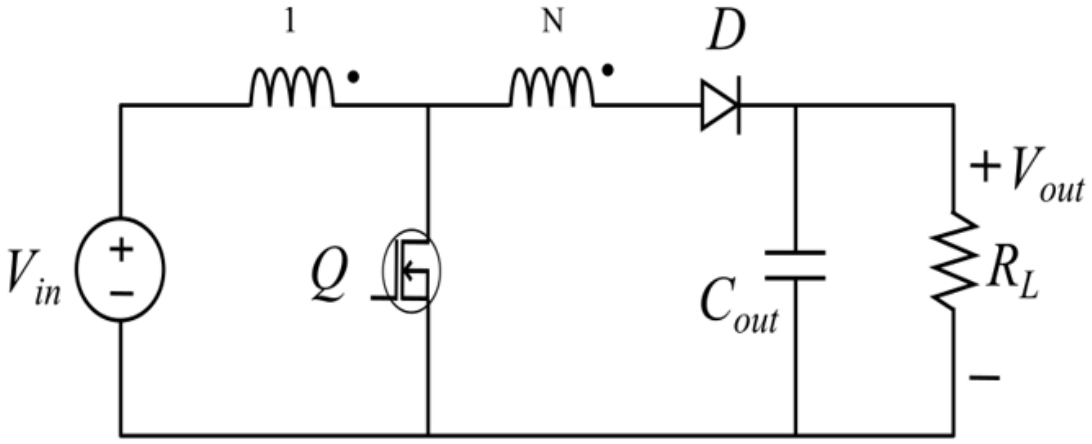


Figure 1 The Tapped Inductor Boost converter consisting of the tapped inductor with a turns ratio N that process power to obtain a high voltage gain at the output

The Tapped Inductor Boost topology can be a simple solution to the high voltage gain requirements. This work explores the possibility that it can be designed to have a performance on par with some commonly used or preferred converter topologies.

DEVELOPMENT AND IMPLEMENTATION OF THE TAPPED INDUCTOR BOOST CONVERTER IN THIS WORK

A Tapped Inductor boost converter can be a possible solution to a high voltage gain requirement, but some challenges needed to be addressed in the design of the converter.

The main design challenge for this converter is to minimize and counter the negative impacts of leakage inductance associated with the tapped inductor. The leakage inductance causes voltage spikes across the primary switch. Resonance between the parasitic output capacitance of the switch (C_{oss}) and the leakage inductance causes this ringing. Ringing by itself isn't harmful until the peak voltage is within the bounds of the voltage threshold of the switch. However, ringing continues until all the stored energy dissipated through the parasitic resistances. Consequently, the stored energy in the leakage inductor is wasted and hence, the efficiency of the converter suffers. Parasitic loop inductance during PCB layout also induces similar problems and hence, needs special attention as well. Techniques to minimize leakage/parasitic inductance are discussed in this work. A loss-less passive snubber can be used to recycle this stored energy in the leakage inductor to further improve the efficiency. This work discusses the use of one such passive loss-less snubber that helps improve efficiency with minimal topological changes.

A complete design procedure is presented. Detailed analysis of each design consideration is discussed. Also, multi-MHz operation of the converter is proposed to minimize the size of the converter and to take advantage of the power semiconductor devices employing WBG (wide bandgap) materials. At multi-MHz frequency, switching losses due to store energy in the capacitors needs to be minimized. Hence, implementing soft switching techniques is also discussed.

Further, at such high frequencies, it is difficult to implement ZVS detection and closed loop control using a microcontroller. A very high frequency clock (possibly in the

order of 500MHz's) is needed. Hence, an analog based control scheme, controlling the "On Time" of the switch based on the ZVS detection is implemented. This is different than a duty cycle or a frequency control scheme and was used for a PFC converter [9]. In addition, a second timer is designed and implemented to kick start the system in case a ZVS condition is not detected. The design and the implementation of the control scheme is discussed.

To understand the converter in detail, the steady state analysis is explained in Chapter 2 assuming it is operated like a Pulse Width Modulated (PWM) converter. This helps understand the working of the converter and its advantages.

Chapter 2: Analysis of a Tapped-Inductor Boost Converter

The idealized Tapped-Inductor Boost Converter [8] works similarly to a Boost converter apart from the additional voltage gain at the output obtained using the tapped inductor. Hence, the analysis is similar to that for a conventional boost converter. The only addition is to model the tapped inductor to simplify this analysis. To study the converter, the tapped-inductor is modelled using a magnetizing inductor and an ideal transformer with a turns ratio 1: N. For a simpler analysis, this model assumes that there is no leakage associated with the tapped-inductor. This can be seen in Figure 2.

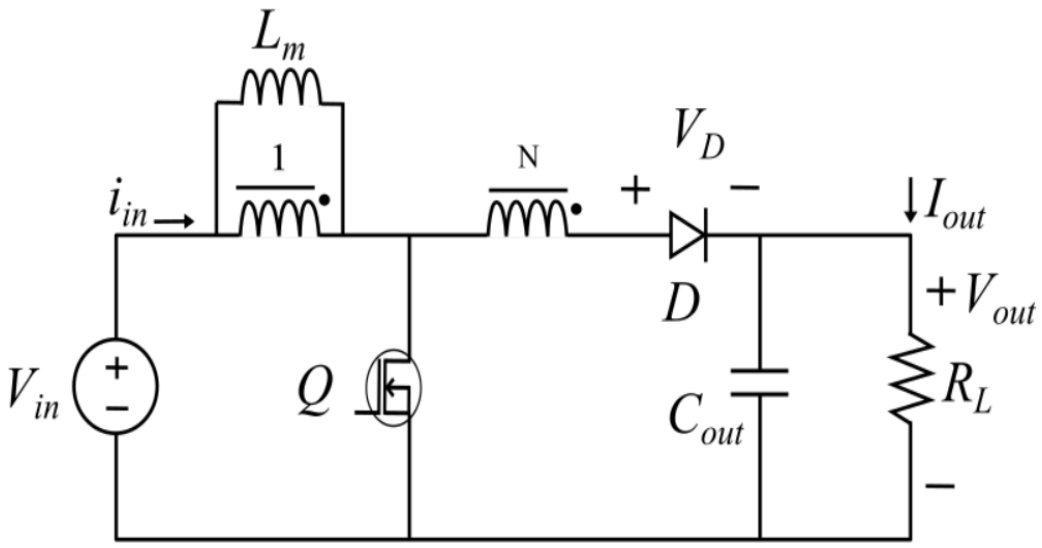


Figure 2: The Tapped Inductor is modelled in the converter using an ideal transformer, a magnetizing inductance, the leakage is ignored during the analysis

This section analyzes the converter in continuous conduction mode (CCM) and in discontinuous conduction mode (DCM) assuming steady state operation. For CCM, the voltage conversion ratio is obtained using the fact that the magnetizing inductor current is periodic. And for DCM, average source current is used to obtain the voltage conversion

ratio. The voltage conversion ratios indicate the advantage of having a tapped inductor to get a higher voltage step-up.

CONVERTER ANALYSIS IN CCM ASSUMING STEADY STATE OPERATION

The analysis assumes that the converter is operating in CCM and is in steady state and hence, the inductor currents are periodic. Each switching state is discussed here in detail.

Mode I [t_0 to t_1]: SWITCH (Q) ON

During this period (refer Figure 3), the primary switch is on, all the input current flows through the magnetizing inductor before returning back to the source through the switch. This magnetizes the magnetizing inductor. The diode is reversed biased. Hence, the secondary side is disconnected from the input. The output capacitor has to supply all the load current. Also, no current flows through the primary or the secondary of the ideal transformer. The voltage across the magnetizing inductor is the same as the input voltage V_{in}.

Hence, the rise in inductor current is given by $I_{m\text{-}rise}$

$$I_{m-rise} = \frac{V_{in} \times (t_0 - t_1)}{L_m} \quad (1)$$

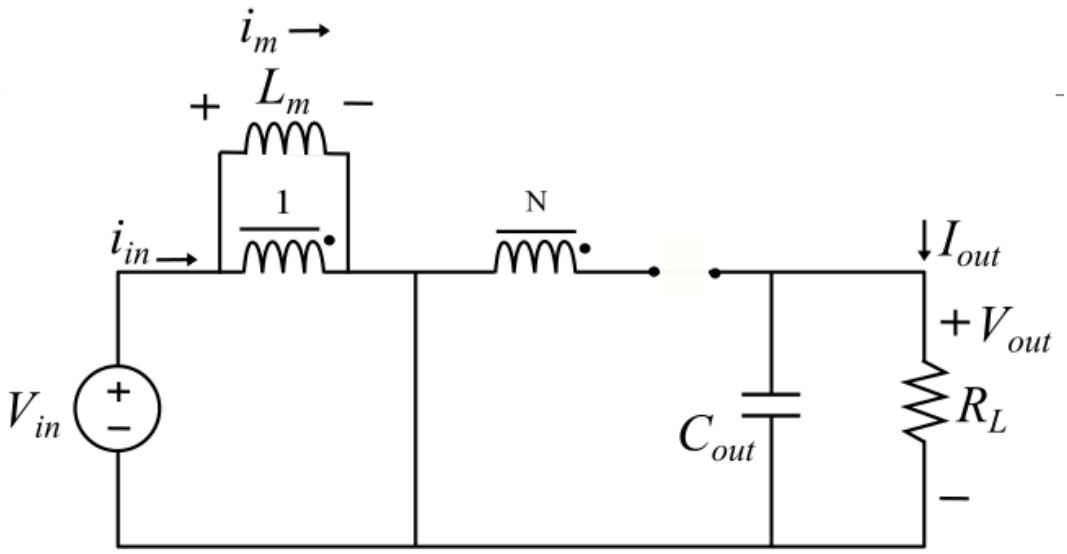


Figure 3: Equivalent circuit of the converter in Mode I, wherein the input is charging the magnetizing inductance and because the diode is reverse biased the output capacitor supplies all the power to the load

Mode II [t_1 to t_2]: SWITCH (Q) OFF, DIODE ON

During this period (refer Figure 4), the primary switch is off. The magnetizing inductor discharges though the primary of the ideal transformer. Hence, the voltage across the magnetizing inductor is given by (2) and the current fall is given by $I_{m\text{-}fall}$

$$-\frac{V_{out}-V_{in}}{N+1} \tag{2}$$

$$\mathrm{I_{m-fall}} = \frac{(V_{out}-V_{in})}{N+1}\,\frac{\times (t_1-t_2)}{L_m} \tag{3}$$

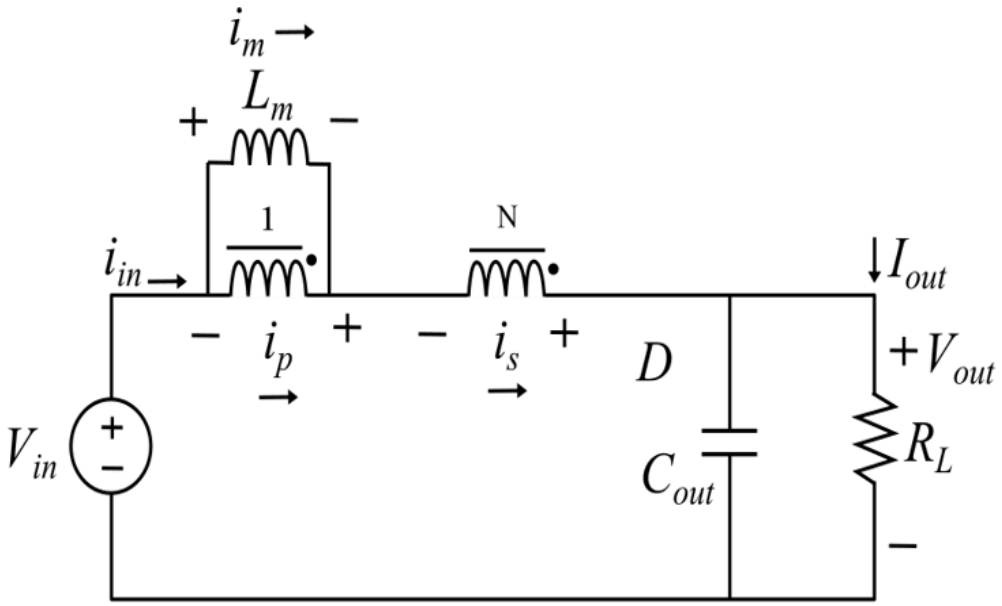


Figure 4: Equivalent circuit of the converter in Mode II, the magnetizing inductor is discharging itself via the primary of the ideal transformer and hence, the stored inductor energy is transferred to the output

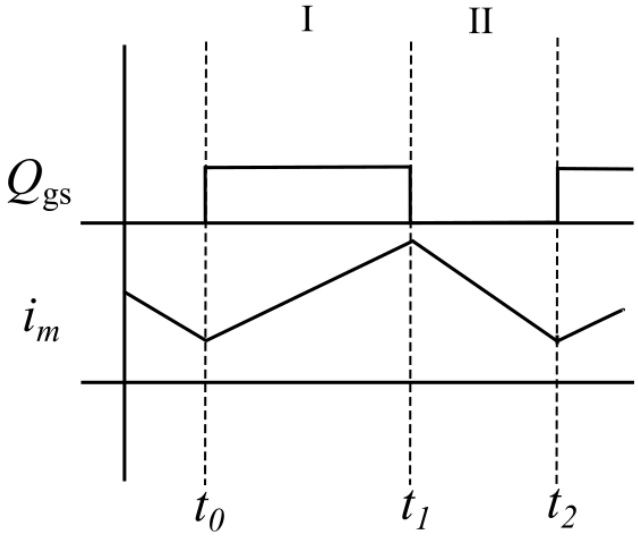


Figure 5: The waveforms showing the magnetizing current in CCM operation, the current in the magnetizing inductor increases linearly when Q is ON and decreases through the output diode when Q is OFF

The magnetizing inductor current waveform is shown in Figure 5. If the converter is operated as Pulse-Width Modulated (PWM) converter, with D being its duty cycle, and is in steady state ($I_{m\text{-}fall} = I_{m\text{-}rise}$). The conversion ratio for this converter is

$$\frac{Vout}{Vin} = \frac{1 + ND}{1 - D} \tag{4}$$

The voltage conversion ratio as given by (4) points towards the advantage of using a tapped inductor. The tapped inductor structure provides an additional voltage gain that depends on the turns ratio N.

As opposed to a regular boost converter, a factor of ND is present in the numerator that provides an additional voltage boost as needed. This clearly indicates that for the same duty cycle, a much higher voltage gain at the output is obtained in a Tapped Inductor Boost converter. A lower duty cycle operation would mean lower resistive loss hence, making the converter practically feasible. Also, the maximum switch node voltage that the primary switch Q has to support is

$$\frac{V_{out} + NV_{in}}{N + 1} \tag{5}$$

This is significantly lower than V_{out}, which is the maximum switch node voltage for a Boost converter. The benefit of lower switch node voltage increases with the increase in turns ratio N of the tapped inductor.

Another approach to discuss the working of the converter is by using the concept of an equivalent inductance. Instead of modelling the tapped inductor, an equivalent

inductance is used instead. The equivalent inductance changes depending on the switch configuration.

When the switch is on, only the primary of the tapped inductor forms a closed circuit with the source since the diode is reversed biased. This can be seen in Figure 6. Hence, the net inductance in the circuit is only due to one turn, and is denoted by L. The current in the inductor rises linearly as the source charges this inductor. The peak energy stored in the inductor during this time period is $E_{pk,1}$

$$E_{pk,1} = \frac{1}{2} L {i_{m-pk}}^2 \tag{6}$$

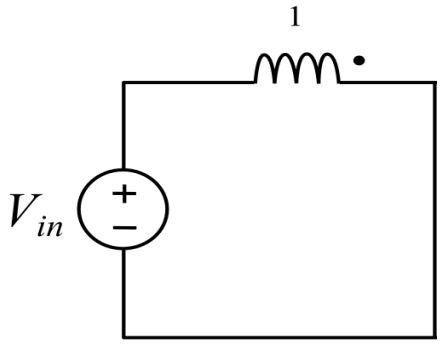


Figure 6 Equivalent circuit during Mode I showing the tapped inductor modelled as an inductor with inductance L; the source charges the inductor and the output capacitor provides all the power to the load as the diode D is reversed biased

When the switch is open, the diode starts to conduct. The primary, the secondary of the tapped inductor, and the source all are in series. This can be seen in Figure 7. The equivalent inductance in this switching cycle is due to (N+1) turns. Hence, the equivalent inductance is given by $(N+1)^2L$. In fact, the higher inductance during discharge is the reason for a higher voltage boost at the output.

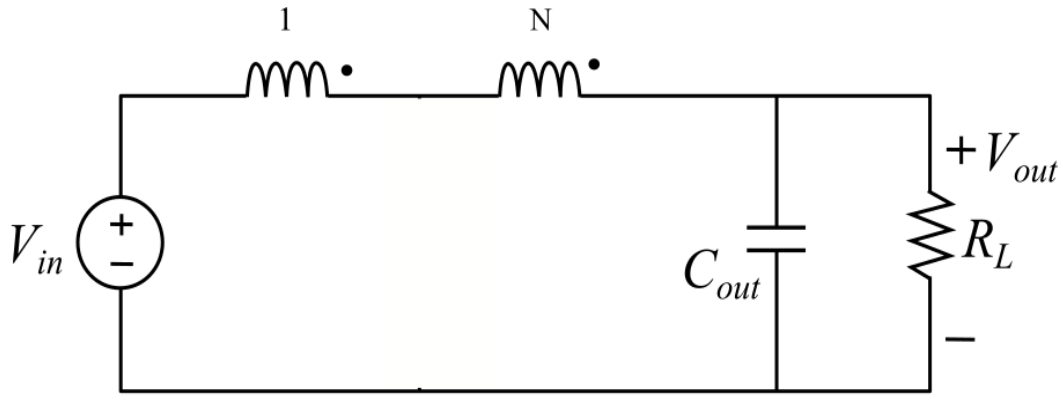


Figure 7 Equivalent circuit during Mode II showing the tapped inductor modelled as an inductor with inductance $(N+1)^2L$, the inductor discharges itself to supply power to the output

The peak energy in the inductor during this part of the switching cycle is given by $E_{pk,2}$, where $E_{pk,2} = 0.5L(N+1)^2I_{in\text{-}pk}^2$. This is at t_1 (refer Figure 8). Energy in an inductor cannot change instantly hence, by continuity, the energy just after t_1 when the switch is off has to be the same as just before t_1 ($E_{pk,1} = E_{pk,2}$) . Therefore, $I_{in\text{-}pk}$ which is, the peak input current when the switch is off is

$$i_{in-pk} = \frac{i_{m-pk}}{N+1} \tag{7}$$

There is a sudden change in inductor current as seen Figure 9. As discussed in chapter 3, this can be damaging to the converter performance when parasitic inductances are included in the analysis. Also, these negative impacts worsen as the leakage inductances increases.

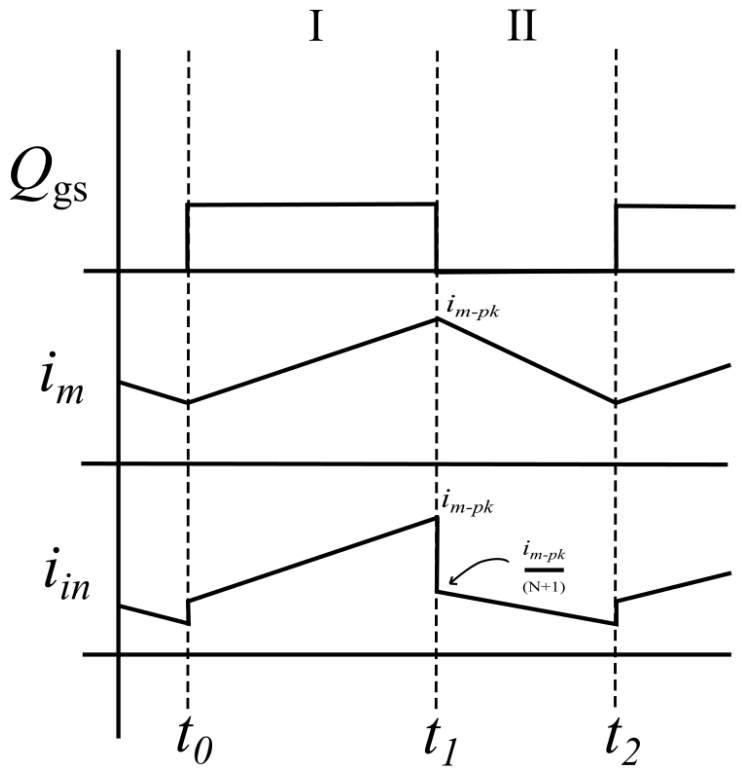


Figure 9 An illustration of the waveforms of the input current that undergoes sudden change each time there is a switching transition; the input current is the same as the magnetizing current when Q is ON

CONVERTER ANALYSIS IN DCM AND STEADY STATE OPERATION

Mode I [t_0 to t_1]: SWITCH (*Q*) ON

Similar to the CCM operation, the switch is on during this period. Hence, input voltage charges the magnetizing inductor, and the output capacitor supplies all the power to the output. The only difference is, DCM operation means the inductor current is allowed to fall to zero before the end of each switching cycle. The converter is operated at a fixed duty D and each switching period is denoted by T. Hence, the rise in inductor current is equal to the peak of the inductor current $I_{m\text{-}pk}$

$$I_{m\text{-}pk} = \frac{V_{in} \times DT}{L_m} \tag{8}$$

Mode II [t_1 to t_2]: SWITCH (*Q*) OFF, DIODE ON

The magnetizing inductor discharges through the primary of the ideal transformer similar to that in case of a CCM operation. But the current is allowed to fall all the way to zero, this is where DCM differs from CCM. The diode conducts during this time period. The current through the diode and the source are the same. The peak of the source current during this period is $I_{in\text{-}pk} = I_{m\text{-}pk}/(N+1)$.

Mode III [t_2 to t_3]: BOTH SWITCH and DIODE OFF

An additional state, during which both diode and controlled switch remains off is obtained as a result of DCM operation. Source supplies no power to the load and hence, the output capacitor has to supply the load.

Assuming 100% efficient operation, input power has to be equal to the output power.

$$V_{in} \times \langle i_{in} \rangle = \frac{{V_o}^2}{R} \tag{9}$$

$$\langle i_{in} \rangle = \frac{1}{2} \frac{(ND+1)DT \times V_{in}}{(N+1)L_m} \tag{10}$$

$$\frac{V_0}{V_{in}} = \sqrt{\frac{2(N+1)L_m}{DT(ND+1)R}} \tag{11}$$

Therefore, it can be seen that a higher N would mean a higher output voltage for the same duty cycle. This concludes that the addition of the transformer provides a higher voltage step-up and helps to process a higher amount of power per cycle for the same duty of operation.

In this work, we propose to operate the converter near boundary of CCM and DCM (called as a Boundary Conduction Mode). The reasons for the same along with other design decisions for the converter are discussed in the following chapter.

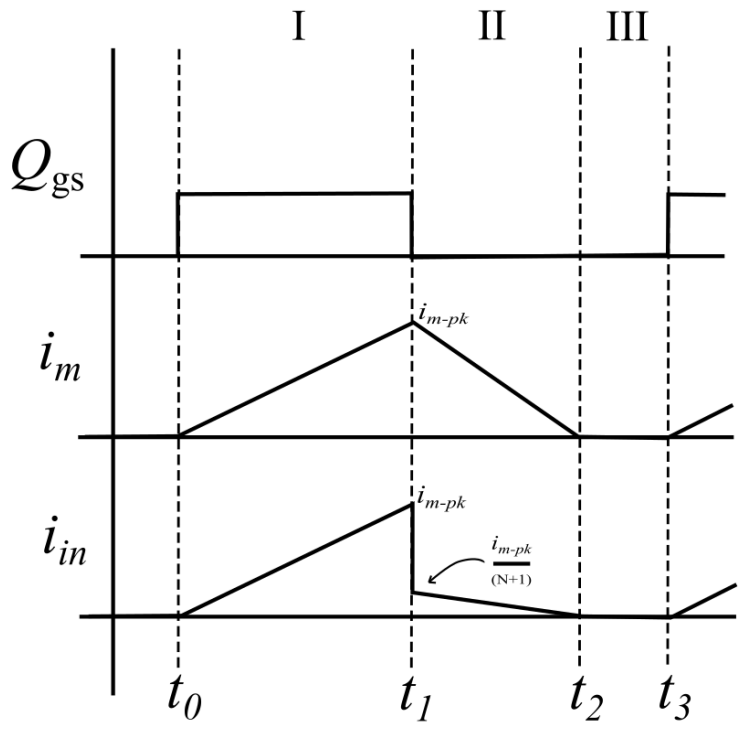


Figure 10 An illustration showing the magnetizing current and the input current in DCM mode, the sudden change in input current is now limited to the turn off transition of Q

Chapter 3: Design for a High Voltage Gain Tapped Boost Inductor Converter

Important design considerations for a 20-400V, 400W Tapped Inductor Boost converter included the mode of operation, the switching frequency, and the transformer. For the transformer, the optimum turns ratio was determined, based on certain tradeoffs, discussed here.

The converter is designed to operate in Boundary Conduction Mode (BCM) as the inductor storage requirement is minimum for a BCM operation. The energy storage requirement is a tradeoff that depends on the ripple ratio. As the ripple ratio for the inductor current increases, the energy storage requirement at first decreases since a lower inductance value is used to process the same amount of power. After a certain ripple ratio, the peak inductor current dominates over the decreasing inductance value, which demands more energy storage. An optimum storage is achieved when the converter is operated in BCM (ripple ratio is 1). This first order analysis ignores the filter capacitors at the input and outputs, since the energy density of the capacitors is assumed to be much higher than that of the inductors.

The converter is chosen to be operated at a multi-MHz frequency. A high-frequency operation is imperative to achieve a high-power density, to maximize the performance of the magnetic material and to have a high control bandwidth. A high frequency means lower energy storage requirement each switching cycle to process the same power, and, hence, higher power density in storage. The performance factor of modern magnetic material are higher in the MHz range. Therefore, it is best to operate at those frequencies to maximize the utilization of the magnetic material. Finally, a higher operation frequency means a faster response to disturbances owing to a faster closed loop control. With these advantages in mind, a multi-MHz operation of the converter is ideal.

High frequency power converter operation is facilitated by the developments in Wide Band Gap (WBG) semiconductor devices. A Gallium Nitride (GaN) based device has a better Figure-of-Merit ($R_{ds,on} \times C_{oss}$) than a similar rated Si based device. Also, the parasitic gate capacitances are much lower enabling faster and efficient switching. Thus, a GaN based MOSFET is an optimum choice for the primary switch.

The design for the transformer is important and is discussed in detail further in the chapter. The major design considerations for the transformer includes, optimizing the turns ratio considering the relevant tradeoffs, design strategies to minimize the high conduction losses especially considering the secondary effects like Skin effect and Proximity effect that are prevalent especially at higher operation frequencies, and finally, minimizing the parasitic leakage inductances that can be damaging to the converter performance.

MAJOR DESIGN CHALLENGES

Multi-MHz operation of the power converter has benefits like high power density, large bandwidth and maximizing the performance of the magnetic materials but there are some challenges to overcome. The major challenges includes losses due to skin effect and proximity effect in the magnetic component that are more prominent as the operation frequency increases. Next major challenge is the energy stored losses in the parasitics. Parasitics like the output capacitance of the MOSFETs and the parasitic inductances due to layout or un-avoidable leakage inductances of the tapped inductor leads to losses that scale directly with frequency. Their direct scaling with frequency can pose a limitation. This section discusses each of these loss mechanism in detail and provides an effective solution to minimize them.

MINIMIZING STORED ENERGY LOSSES DUE TO C_{oss} OF THE MOSFETS

In a BCM operated Tapped Inductor Boost converter, each time the MOSFET is turned-on, the parasitic output capacitance of the MOSFET (C_{oss}) discharges through the switch. This leads to a $\frac{1}{2}$ CV^2 loss. Further, this loss scales directly with frequency. This is referred to the turn-on switching loss due to stored energy. This section identifies this stored energy loss in the capacitor during the turn-on process and provides a solution for the same.

ZERO VOLTAGE SWITCHING

To eliminate these turn-on switching loss, the switch should be turned on when the voltage across the C_{oss} capacitor is zero. This is called as the "Zero Voltage" turn on. To achieve a Zero Voltage Switching (ZVS) or in particular a ZVS turn-on, a valley switched converter operation in proposed.

In Valley Switched mode, towards the end of the switching cycle when the current through the magnetizing inductor is zero, the magnetizing current is allowed to resonate with C_{oss} capacitor. The equivalent circuit for this duration is shown in Figure 11. During this period, because the magnetizing inductor is fully discharged it cannot force current through the diode anymore, the diode can no longer conduct and can be ignored during the resonant period. Also, the switch is off hence, is represented only by its output capacitance. The resonance between C_{oss} and magnetizing inductance means the switch node voltage will oscillate about V_{in}. Ideally, the switch node voltage should oscillate such that the switch node voltage rings down all the way to zero. If the switch is turned-on right when $V_{sw,node}$ is zero, we get a ZVS turn-on.

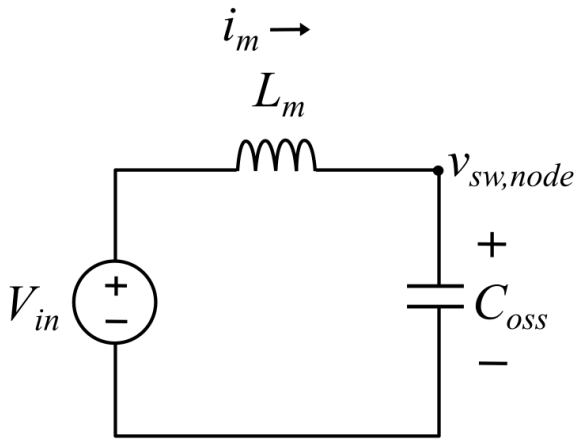


Figure 11 An equivalent circuit in Mode III (the resonant period) wherein, the magnetizing inductance resonates with the C_{oss} of the MOSFET; the switch node voltage oscillates about V_{in} that induces a possibility of a ZVS turn-on

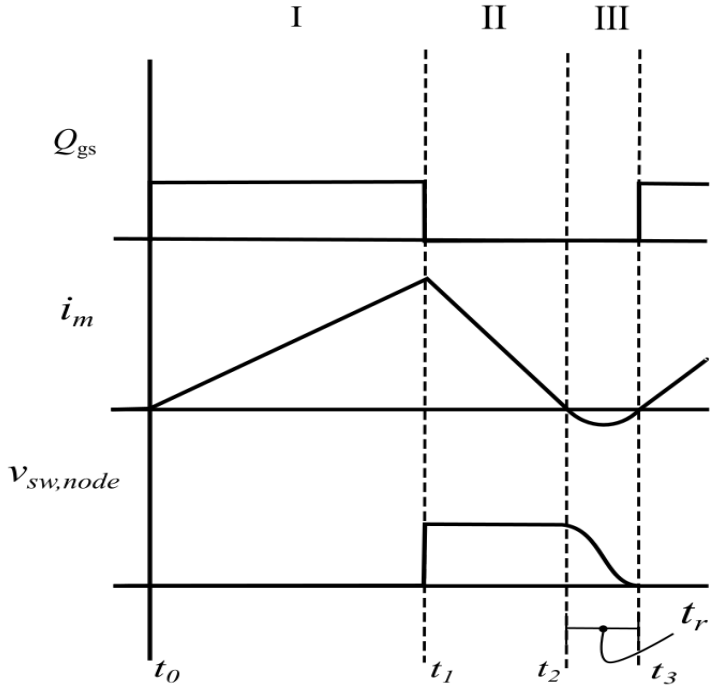


Figure 12 An illustration of the switch node and the magnetizing current waveforms that highlight the commutation of the switch node voltage during the resonant period (Mode III) facilitating a ZVS turn-on for the MOSFET

It should be noted that for the switch node voltage to commutate to zero, there should be a minimum $V_{sw,node}$ voltage at the start of the resonating cycle. The $V_{sw,\ node}$ should at least be equal to $2V_{in}$ to help the switch node voltage commutate all the way to zero.

Maximum switch node volage $V_{sw,\ node}$ is given by (5). Hence, this puts a limit on the maximum allowable turns ratio for the tapped inductor

$$N \leq \frac{V_{out}}{V_{in}} - 2 \tag{12}$$

It is important to note that the control mechanism should be able to turn on the MOSFET as soon as a Zero Voltage is detected on the switching node. This is important because beyond this, if the voltage across the switch goes negative, the body diode starts conducting. Body diodes of FETs have high forward voltage drops, current conduction through them is a lossy process. The resonant time period is t_r

$$t_r = \frac{\pi}{\sqrt{L_m C_{oss}}} \tag{13}$$

Hence, it can be seen that the C_{oss} should be minimized to have a very short resonant period. However, a smaller C_{oss} value means a larger $R_{ds,on}$. Hence, the switch selection process should be optimized accordingly.

As a first order approximation, the above resonant time period works. However, it should be noted that the diode during the resonant period should be modelled by its output capacitance C_d. Hence, the diode capacitance is added in parallel with the C_{oss} capacitor as an equivalent capacitance $C_{eq,d}$

$$C_{eq,d} = C_d(N+1)^2 \quad (14)$$

Hence, C_{oss} is replaced by C_{eq} for resonant time calculations. The modified resonant time is given by

$$t_r = \frac{\pi}{\sqrt{L_m(C_{eq,d} + C_{oss})}} \quad (15)$$

It should be noted that apart from helping with the ZVS, the resonant time is detrimental to the efficiency of the converter as no power is processed to the output during this time. The resonant time increases with increasing C_{oss} of the MOSFET. Hence, the switch selection is not a straight forward process but a tradeoff between conduction loss and resonant time. The actual loss calculation during the resonant period is a complex process. To simplify switch selection process, it is reasonable to assume that the t_r cannot be more that 15% of the switching period. This provides a limit for C_{oss} and hence, $R_{ds,on}$ can be selected using the FOM of the switch.

Lastly, as part of the control circuitry, a mechanism is needed that monitors the switching node voltage continuously. As soon as the switching node hits zero, it should trigger a gate drive signal that turn the MOSFET back on. Chapter 4 discusses this control scheme in detail.

MINIMIZING STORED ENERGY LOSSES DUE TO LEAKAGE IN TAPPED INDUCTOR

Leakage inductances are unavoidable in a practical tapped-inductor. Considering a practical design, it is impossible to eliminate the self-flux linkage of the primary or the secondary winding. This contributes to leakage inductances. To study their effects in detail,

it is easier to represent them in a circuit model. Since, these store energy in form of magnetic fields, they are modelled as inductors. The primary leakage inductor L_{lp} models the energy stored due to flux that links only the primary winding. Similarly, the secondary leakage inductor L_{ls} models the energy stored due to flux that links on the secondary of the tapped-inductor. Refer Figure 13.

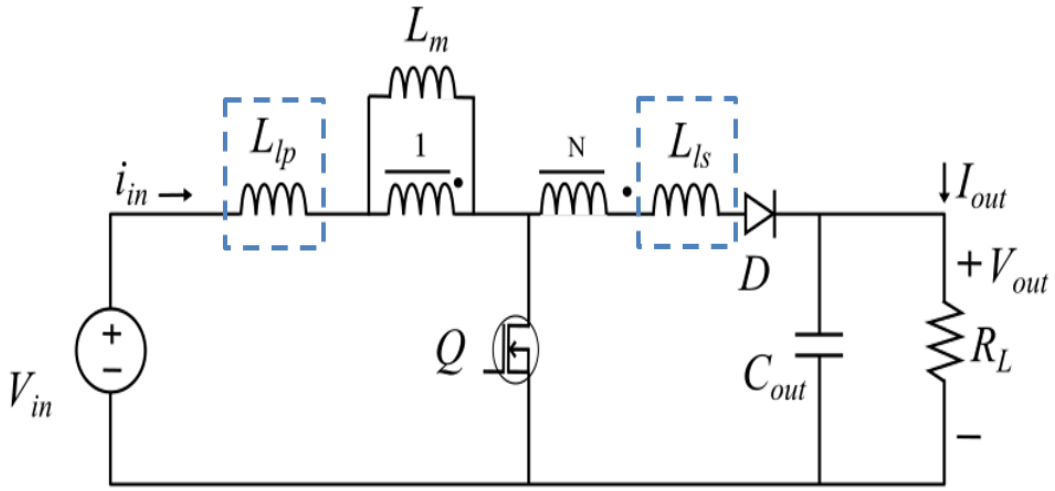


Figure 13 A converter circuit consisting of a more complete model of the tapped-inductor; the addition of the leakage inductances help illustrate the high stored energy turn-off losses that might hamper the converter efficiency

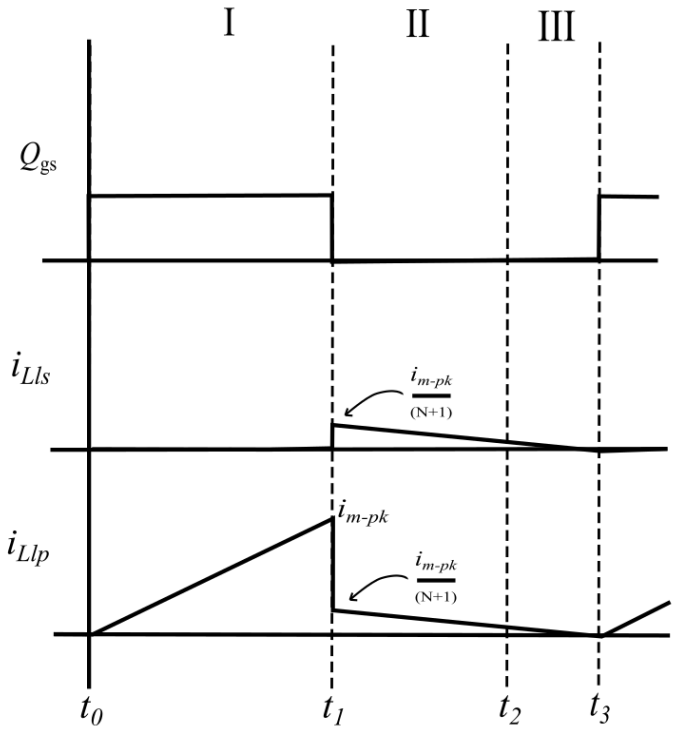


Figure 14 Illustration of the primary and the secondary leakage inductor current waveforms highlighting the sudden drop in currents during the turn-on transition in BCM operated converter

The current through the L_{lp} is the same as source current and the current through L_{ls} is the same as the diode current. The currents in L_{lp} and L_{ls} are shown Figure 14. It can be seen that the current in L_{lp} undergoes a sharp drop when the switch is turned off. Similarly, the current in L_{ls} undergoes a sharp jump during the same switching instance. The currents in the parasitic inductances are forced to change instantly due to circuit operation. This certainly is unnerving. The sudden current drop in L_{lp} leads to an energy loss given by (16) and a sudden jump in L_{ls} current leads to energy loss given by (17). For numerical context, a 5% leakage inductance to magnetizing inductance ratio, means approximately 10% increased losses. This results to a nasty hit on the efficiency thus, an

effective solution to recycle this energy back to the source or the load is a must. These leakage losses are given by $P_{loss,Llp}$ and $P_{loss,Lls}$.

$$P_{loss,Llp} = \frac{1}{2} L_{lp} \left(\frac{N}{N+1} \times i_{m-pk} \right)^2 \quad (16)$$

$$P_{loss,Lls} = \frac{1}{2} L_{ls} \left(\frac{i_{m-pk}}{N+1} \right)^2 \quad (17)$$

It is the exact dual of the $\frac{1}{2}$ CV^2 losses in the C_{oss} capacitors during the turn-on process as discussed earlier. Together they are referred to as the stored energy switching losses. To catch up with the sudden drop in current during turn off, the primary leakage inductor L_{lp} releases all its energy in a sudden bust of voltage to discharge itself. If it were an ideal switch (with no parasitic capacitances), this voltage would have been very high and would have certainly breached the breakdown voltage of the switch. However, the presence of C_{oss} of the MOSFET dampens this voltage. But since the energy stored in the L_{lp} resonates with the C_{oss}, there is significant ringing at the switching node during. A smaller C_{oss} means lower damping and hence, a higher ringing resulting in breaching the breakdown of the voltage threshold of the switch. One solution could be to add snubber capacitors in parallel with C_{oss}, but this increases the resonant time significantly as seen in (15). Generally, the turn-off losses are ignored in most converter analysis without any noticeable efficiency drops, but for this converter it is impossible to ignore them.

Also, a frequency of 2MHz is chosen as the operating frequency of the prototype converter. For a 2MHz frequency, the required magnetizing inductance for a BCM operated 20-400V, 400W converter is 105nH.

It should be noted that a 105nH magnetizing inductance is a very small inductance value, and it is very difficult to limit leakage inductances below 5% of the magnetizing inductance. Hence, apart from design strategies to minimize leakage inductance, it is important to design a circuit based solution to recycle the energy stored in the parasitic inductances. Hence, the design of a passive lossless snubber is discussed [10].

SNUBBER DESIGN

A simplest snubber design is to add capacitor in parallel with the MOSFET to dampen the ringing by providing a storage for the leakage energy in L_{lp}. However, this leads to higher turn on losses. This is because every time the switch is turned on, the snubber capacitor discharges through the switch leading to $\frac{1}{2}$ CV^2 loss. If ZVS is obtained by allowing the snubber capacitor to resonate with the magnetizing inductance the resonant time, as given by (15), will be very high. Hence, a ZVS turn-on in this case will limit energy storage losses, but a high resonant time will still limit the operation frequency. Also, the resonant current doesn't supply power to the load leading to inefficient converter operation.

The solution to this problem is, the addition of a loss-less passive snubber as shown in Figure 15[10]. This passive snubber circuit includes a snubber diode in addition to a snubber capacitor. The snubber diode conducts only in the forward direction meaning that the snubber capacitor can only discharge through the output. This eliminates the $\frac{1}{2}$ CV^2f_{sw} losses due to instant discharging of the capacitor through the switch. The snubber capacitor acts as an energy storage element allowing leakage inductors to dump its energy into them. The snubber diode ensures that the snubber capacitor can release this dumped energy only to the output. Hence, ensuring that the energy stored in the leakage inductors is recycled to the output and doesn't contribute to loss.

The output voltage and the maximum voltage across the snubber capacitor are given by V_{out} and V_c respectively. These can be obtained by performing volt-sec balance across L_m and L_{lp}. The leakage is expressed using the coupling coefficient k.

$$V_{out} = \frac{V_{in}[D(k + N - 1) + 1]}{(1 - D)} \tag{18}$$

$$V_c = \frac{V_{in}[D(1 - k)(N - 1) + 1]}{(1 - D)} \tag{19}$$

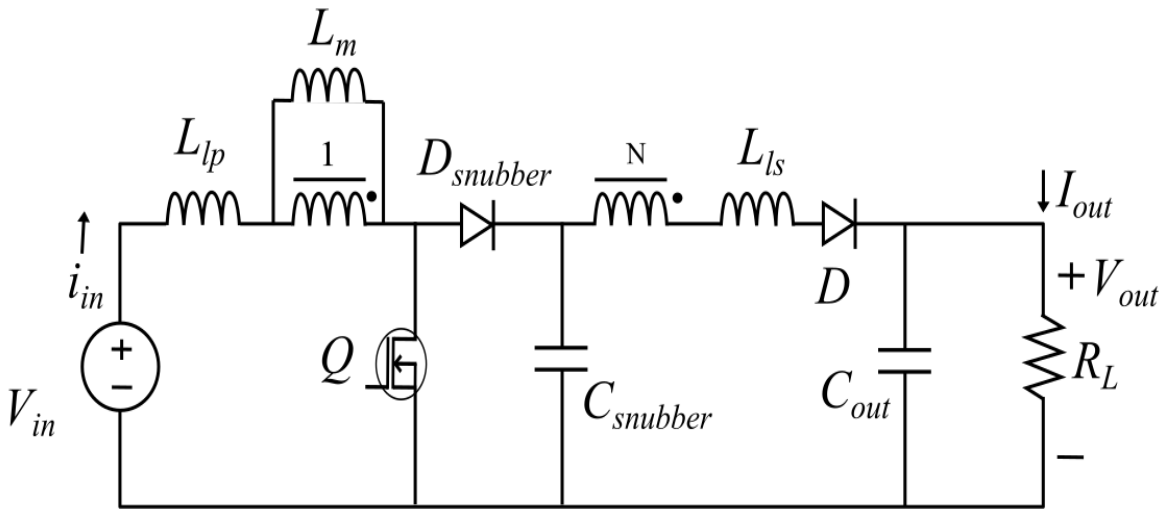


Figure 15 A passive loss-less snubber is incorporated in the converter to recycle the energy stored in the leakage/parasitic loop inductance

The maximum voltage across $D_{snubber}$ is

$$V_{diode,max} = V_c + \frac{i_{m-pk}(1 - D)}{2\, C_{snubber}(N f_{sw})} \tag{20}$$

The maximum voltage the diode has to support is the same as the maximum voltage across the snubber capacitor, this is also equal to the maximum switching node voltage.

A higher leakage results in a higher switch node voltage (as seen by (19)) and hence, a switch with a higher breakdown voltage is needed. The bottom line is, minimizing the leakage inductance is still a very important step to the design process. Even though having a passive loss-less snubber recovers the leakage energy, the best performance of the converter is still on the table up for grabs. Hence, design process to minimize leakage/parasitic inductances is very important.

INDUCTOR DESIGN

The first important design consideration is the turns ratio of the tapped inductor. A higher turns ratio results in a lower duty cycle and lower voltage switch stresses for the same voltage gain. This can be seen in (5). However, there is a tradeoff. A higher turns ratio results in decreasing voltage stress but a higher peak current through the switch. Hence, there is an optimum turns ratio. As seen in Figure 16, the optimum point is at turns ratio = 18.

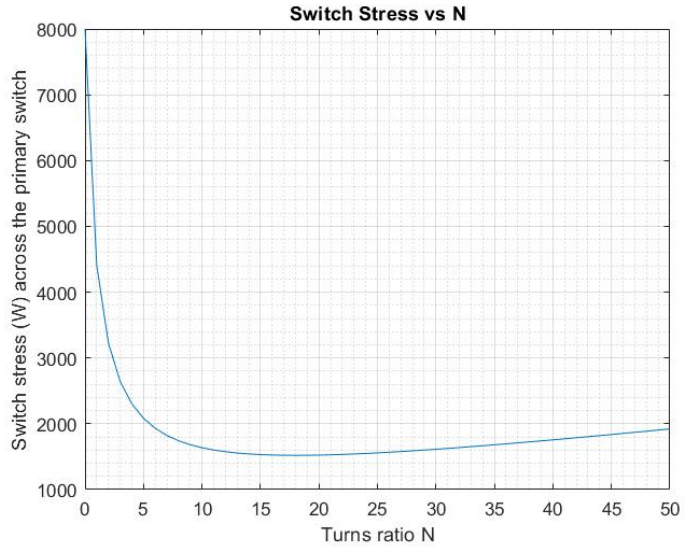


Figure 16 The switch stress vs turns ratio plot illustrating the optimized turns ratio (N = 18) which is a tradeoff between lower voltage stress and the higher peak current as N increases; The decrease in switch stress in not prominent after a turns ration of 10

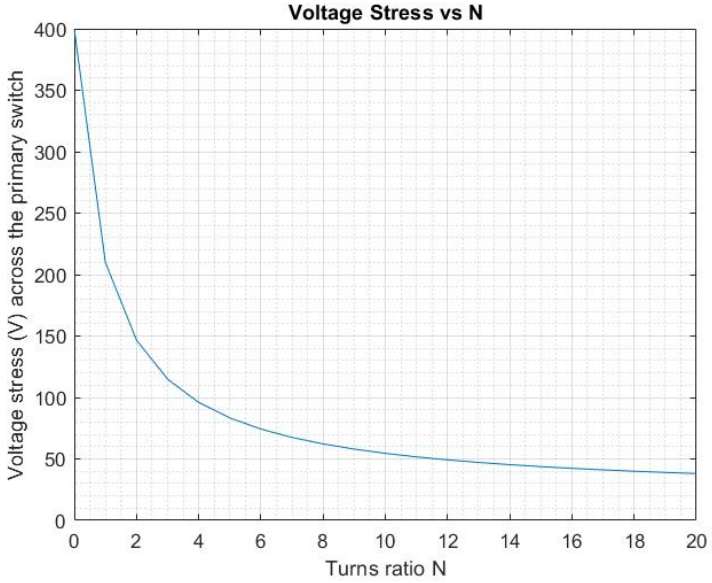


Figure 17 Voltage switch stress as a function of the turns ratio, a higher turns ratio would decrease the voltage stress significantly with the added advantage becoming less prominent at high N

However, as the turns ratio increases the voltage blocking requirement for the output diode ($V_{diode,max} = NV_{in} + V_{out}$) increases .

A secondary maximum limit on the turns ratio is the ZVS condition. To obtain a ZVS turn on for the primary MOSFET, the converter is operated in Valley Switched Mode (as discussed in the earlier section). To obtain a ZVS turn on, the maximum allowable turns ratio is

$$N_{max} = \frac{V_{out}}{V_{in}} - 2 \tag{21}$$

From Figure 16, the decrease in switch stress is not very high after N = 10. Also, the voltage stress doesn't significantly increase to impact the switch selection process. Hence, the turns ratio for the tapped inductor is chosen to be 10.

To minimize the leakage and the conductor losses due to proximity effect, interleaving the primary and the secondary windings is an ideal solution as shown in Figure 18. The primary winding is divided into N parallel paths (N = 10 in this case) and is interleaved with the secondary winding to minimize proximity losses and decrease coupling by reducing opportunity for self-linking flux. Furthermore, using Litz wire for primary and the secondary winding is necessary to minimize conductor losses at such high operating frequencies.

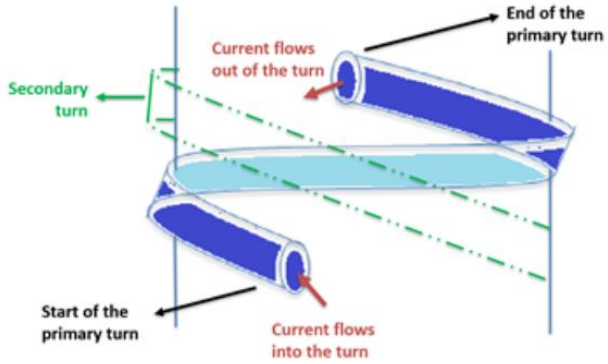


Figure 18 Interleaving the primary and the secondary as shown helps minimize leakage that's critical to improve converter performance

PCB DESIGN

As discussed earlier, it is important to minimize parasitic inductances to minimize energy stored losses. Layout can be a source of high loop inductances if not managed properly. To minimize the inductances due to high frequency, high current loops, vertical loops are preferred over planar loops.

An electrical loop that has high frequency currents flowing through it produces time varying flux. The problem here is two folds. These parasitic inductors have self-coupling flux that results in self-inductances. It can also couple inductively with other loops contributing to mutual inductance. The best strategy to minimize these inductances is to minimize the flux linkage or in other works maximize the reluctance to the flux path. To maximize the reluctance, the loop can be thought as an infinitely long solenoid. Hence, we need to minimize the area of the flux path and maximize the flux path length. This is done by using Vertical loops. Hence, vertical loops should be preferred over planar loops.

Next, it is important to start laying out the PCB starting with the high priority loops. High priority loops are the ones that carry high frequency, high power currents. Parasitic

inductance affect these loops the most. Hence, it is important to ensure the loop inductances of the high priority loops are minimized.

To identify the high priority loop in the converter, we want to start with the power stage of the converter. This is because, they are most likely to have both high frequency and high power. Switching loops are one's that carry the high frequency and high power. Next target is to identify the high priority loops.

The converter is divided into three loops as shown in Figure 19.

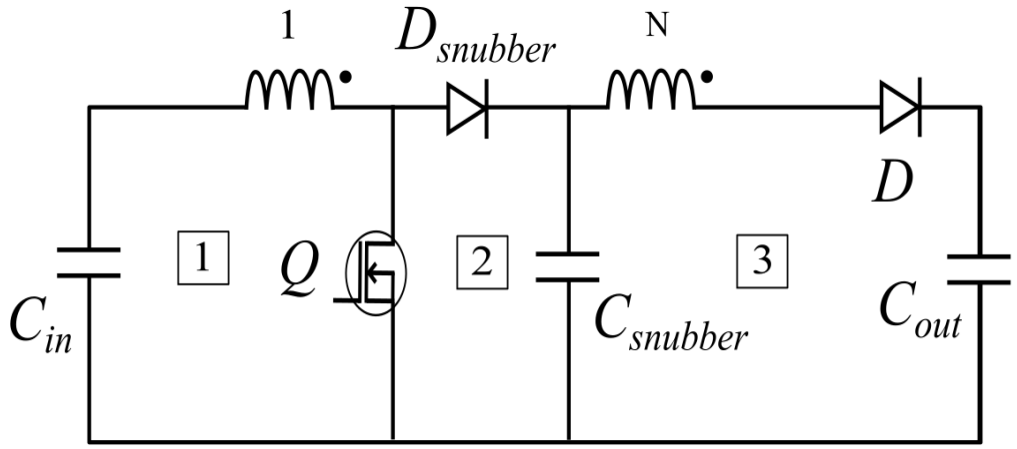


Figure 19 Circuit schematic showing the high current high frequency switching loops indicated by their priority while laying them out on a PCB

Loop 1 consists of very high power currents at the switching frequency. Loop 2 consists components that have high currents but are at even higher frequency as they are discontinuous. A sample vertical loop layout has been shown in Figure 20.

However, because the magnitude of currents is higher in loop 1 and it is now well documented that minimizing the loop inductance of Loop 1 should be prioritized. Next, on the list is loop 2 followed by loop 3 that has high frequency continuous currents but are lower in magnitude.

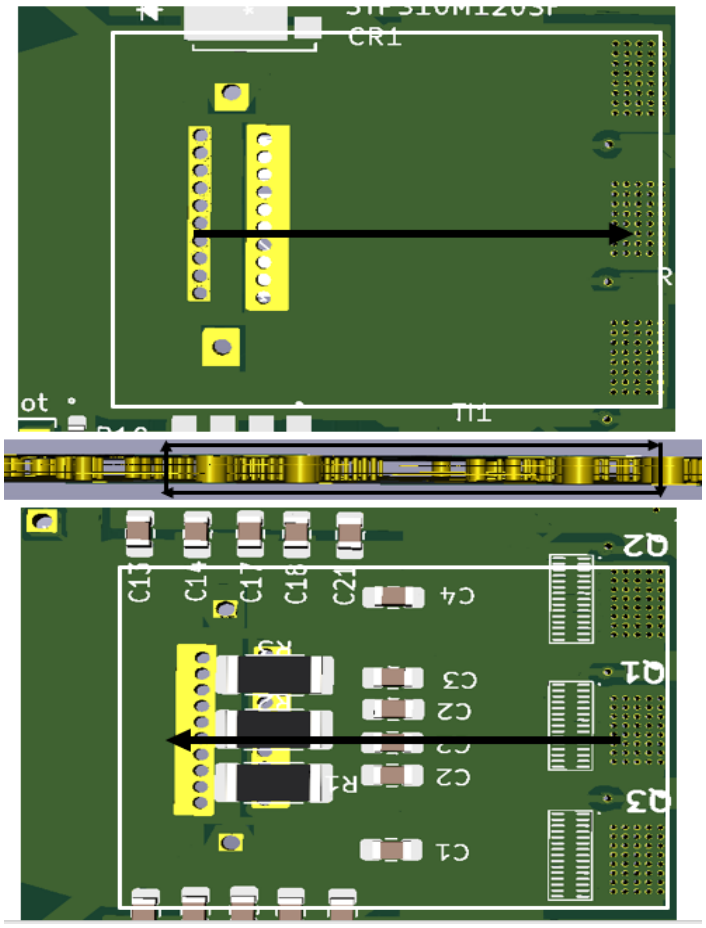


Figure 20 A sample vertical loop for switching loop 1

After laying out the three switching loops, the next high priority loop is the gating loops since, they can have very high burst of current required to charge/discharge the FET gates during each switching cycle. Hence, the gating loops should be kept as small as possible. Gating loops are particularly important in the case of GaN transistors which have high sensitivity to ringing gate voltages.

Next, on the list, will be analog circuitry. Analog control signal are generally sensitive to capacitive coupling and hence, should be kept away from switching nodes. It

is also possible to shield sensitive analog tracks using ground layer. Laying out the digital tracks should be left for the last.

Chapter 4: Controls

To achieve ZVS, in particular a zero voltage turn on, a dedicated module is needed that continuously monitors the switch node voltage. This is needed to identify the zero voltage instant and to generate the switching signals accordingly.

Analog circuitry is preferred over using a microcontroller for this job. Due to the primary leakage inductance, which resonates with the C_{oss} of the MOSFET, the switch node voltage has very high frequency oscillations. Hence, for a multi-MHz operation, very fast sampling is required meaning a very high central clock frequency (>600MHz) would be needed. Hence, using analog control is a more reasonable option.

The control discussed here has been previously used in a PFC converter [9]. The only control variable that controls the output voltage is the "On Time" of the MOSFET. The MOSFET switch backs on only when ZVS condition is detected so, in a sense, there is no control on the off time of the switch. This is called as "On Time" control as referred to in [9]. In addition, a turn off timer is designed that ensures the system runs normally in case a ZVS is not detected.

Refer Figure 21. The ZVS detection circuit monitors the switch node voltage to check for zero crossings. The ZVS reference (REF_{ZVS}) is generated from a 5V DC rail using voltage divider. Once a ZVS is detected, the MOSFET is turned on. At the same time, a ramp timer (On Timer) increases linearly until it reaches REF_{TMR}. This resets the timer and generates an appropriate signal to turn the MOSFET off. An analog compensator controls this REF_{TMR}. REF_{TMR} is a proxy for controlling the on time of the switch. It is important to note that the converter is neither a variable frequency converter nor a PWM

converter. The only control variable to control the output voltage of the converter is the "on time" of the switch. The switching waveforms can be seen in Figure 22.

Additionally, an off timer is designed, to ensure the converter continues to process power in case no ZVS is detected. In theory, the off timer is never needed if the switch node voltage commutates down all the way to zero. But in practice, during a transient operation, it is possible that the switch node voltage never commutates to zero (because the output voltage is not high enough for a ZVS condition). In this case, it is important to have a circuitry that kicks the system back into operation by turning the switch back on. The off-timer performs this job. It turns the switch back on after a certain duration (off time) if no ZVS is detected within this time period, refer Figure 23. When off timer is needed, the converter is hard-switched, therefore it's important to limit the operating frequency. This is done by setting the off timer ramp much slower than that of the on timer. Implementing the off time as discussed, ensures that it never interrupts a normal ZVS turn on incase it's possible.

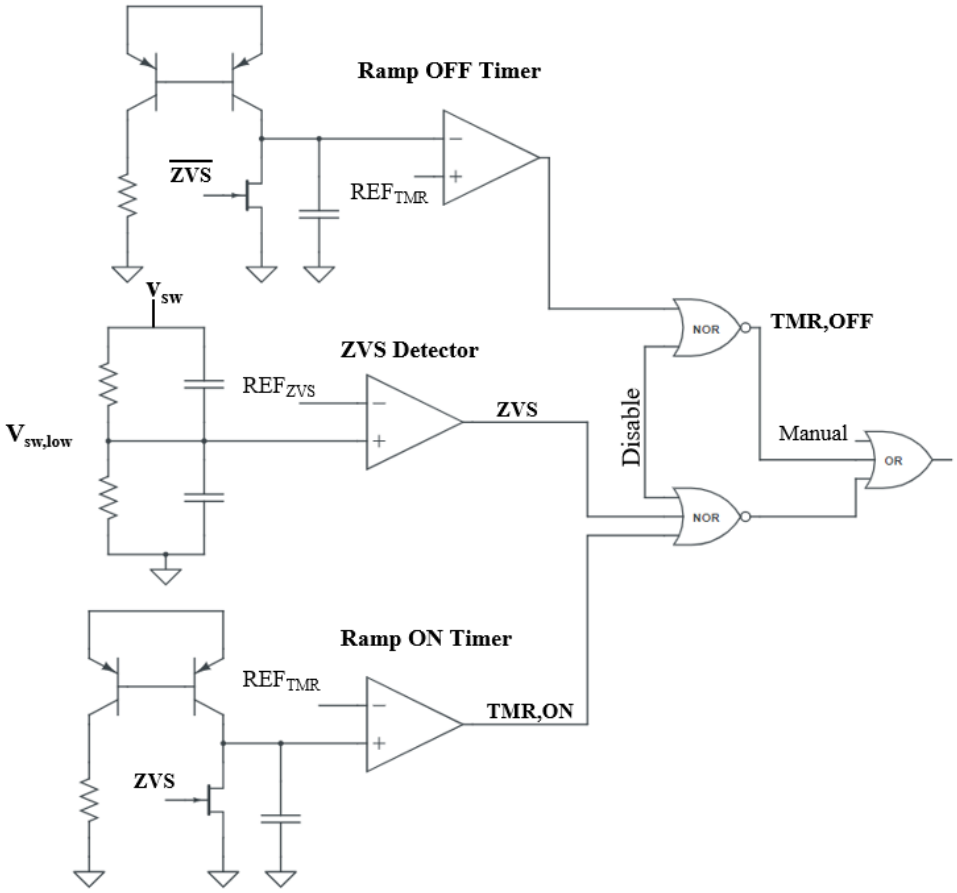


Figure 21 Analog Based control circuit that turns the MOSFET on when a ZVS condition is detected; additional a Ramp Off timer is implemented that the converter runs as process power incase no ZVS condition is detected

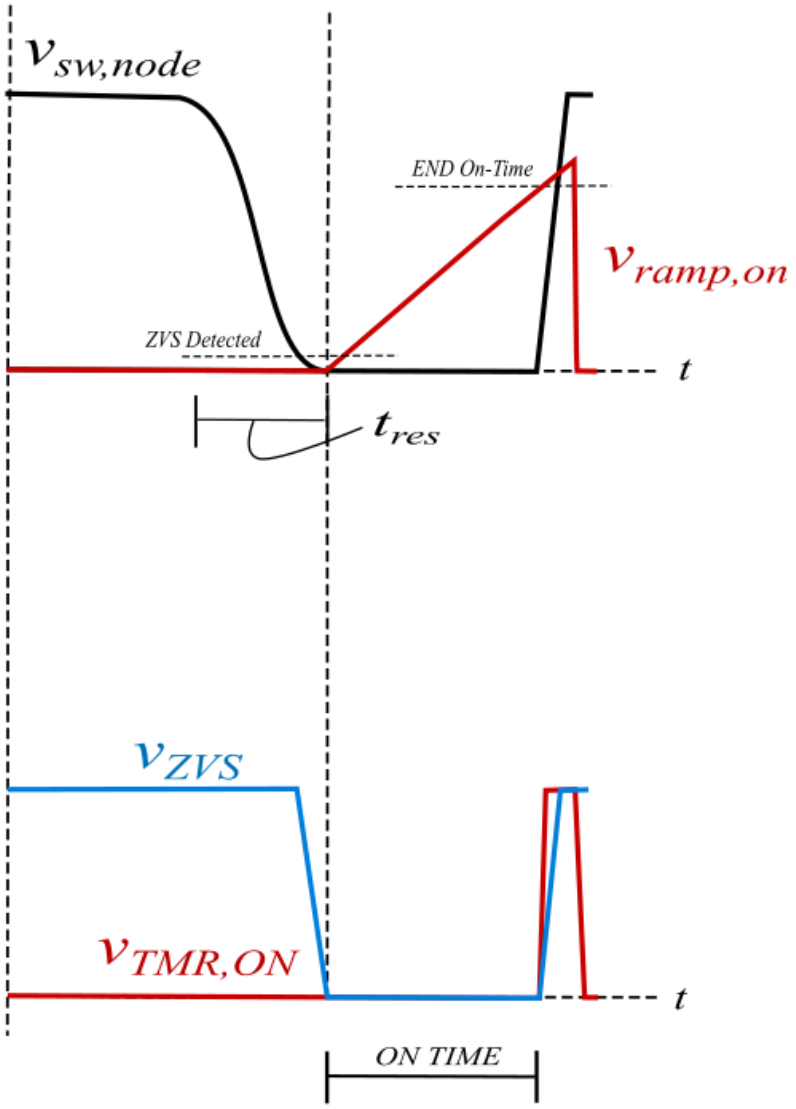


Figure 22 Illustration of the waveforms in the analog control circuit showing how a ZVS detection triggers a ramp,on timer. The reset of this timer triggers a signal that turns off the switch. The ZVS detector circuit it reset and hence, the cycle is repeated at the detection of ZVS condition

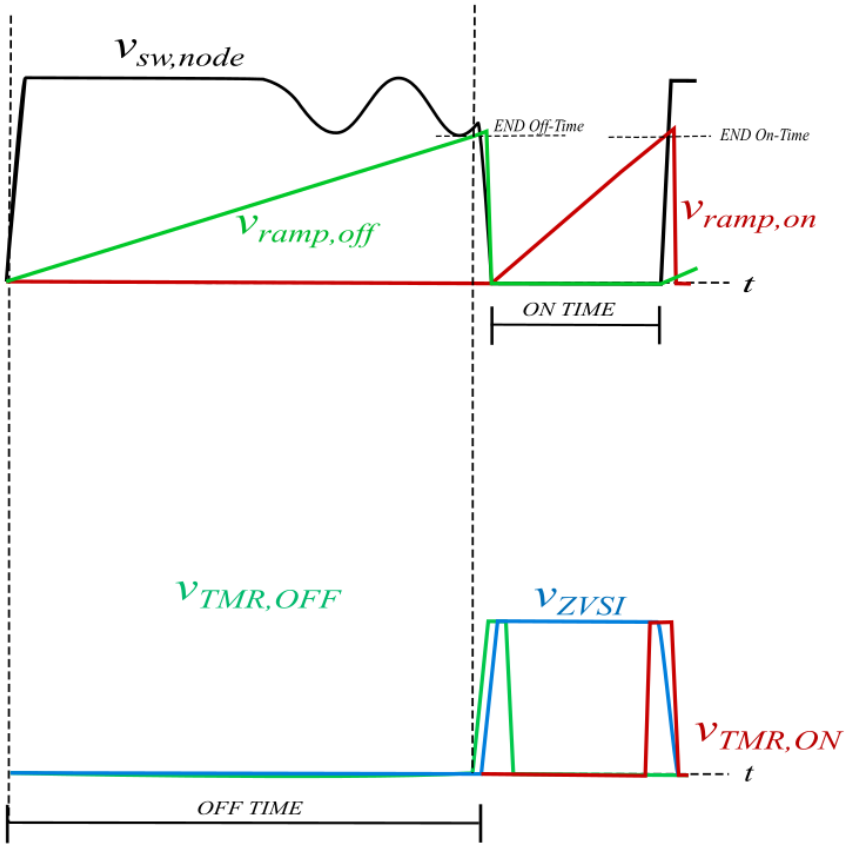


Figure 23 An illustration of the waveforms in the analog based control circuitry when a ZVS condition is not detected; the turning off of the switch triggers a ramp off timer that ensures the switch is turned back on after a certain duration if no ZVS is detected

Both On timer and Off timer comparators are controlled by the same reference signal REF_{TMR}. This signal can be generated by a digital based compensator. For the prototype, an analog compensator is used to generate the reference signals. Next section discuss the process to obtain a small signal model of the converter that's needed to design the compensator.

SMALL SIGNAL MODEL

The small signal model is developed assuming the converter is operated in BCM. The averaged state space equations are obtained assuming variations in the on time t_{on}, the input voltage V_{in}, and the output voltage V_c are much slower than the switching time period over which they are averaged.

$$\frac{d < i_L >}{dt} \cong 0 \tag{22}$$

$$\frac{d < V_c >}{dt} \cong \frac{< i_D >}{C} - \frac{V_C}{RC} \tag{23}$$

where,

$$< i_D > = \frac{1}{2TL} \frac{{V_{in}}^2 {t_{on}}^2}{V_c - V_{in}} \tag{24}$$

Following the process of linearization, the small signal transfer function of the plant is :

$$G_{ol} = \frac{G_{DC}}{\left(\frac{s}{w_p} + 1\right)} \tag{25}$$

where,

$$G_{DC} = \frac{R{V_{in}}^2 t_{on}}{TL(V_{out} - V_{in})} \tag{26}$$

$$w_p = \frac{(2V_{out} - V_{in})}{RC(V_{out} - V_{in})} \tag{27}$$

Since the converter is operated in BCM, the average inductor current is approximately zero and hence, the plant has only one pole and no RHP zeros. This is because there is no memory to the inductor meaning, it is allowed to return to zero each switching cycle independent of the control input. Hence, operating in this mode simplifies the controls by eliminating the RHP zero.

COMPENSATOR DESIGN

The small signal model of the plant has a single pole. An ideal loop gain transfer function has a single pole at dc. A single pole at dc ensures maximum gain possible and a cross-over at -20dB slope. Hence, the compensator requirements are that it should have a zero that's able to cancel the plant pole and has a pole at dc. In addition, a second pole after the crossover frequency is needed to ensure that it compensates for any unmodelled left half plane (LHP) zeros that may present itself due the ESR of the output capacitors. Generally, the ESR of the ceramic capacitors are very low and it's safe to assume that any LHP zero due to them will only be after the crossover. The second pole also helps in achieving a Gain Margin of about 60˚. This GM ensures that the response is fast enough and not overdamped. Hence, the compensator chosen to implement the above requirements is a type II analog compensator as shown in Figure 24. In addition, to prevent saturation of the comparator output to $+V_{cc}$, a Zener diode is added in parallel with the feedback branch to function as an anti-windup for the integrator.

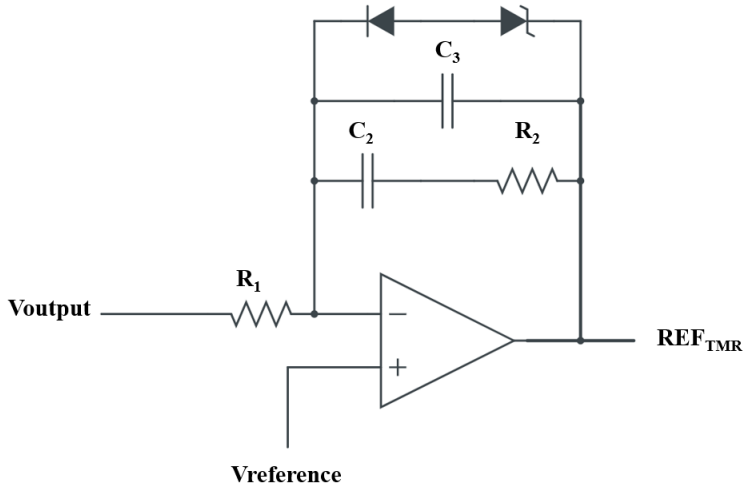


Figure 24 An Op-Amp based Type II Analog Compensator to generate REF_{TMR} that controls the on time of the switch based on the error in the output voltage with respect to the reference output voltage

The transfer function for the compensator is $G_c\,(s)$

$$G_c(s) = \frac{1 + C_1R_2s}{(C_1 + C_3)R_1s + C_1R_1C_3R_2s^2} \tag{28}$$

Assumptions while designing the compensator,

$$C_1 > C_3 \tag{29}$$

$$R_2 > R_1 \tag{30}$$

For low frequencies, because $C_1 > C_3$ the C_3 branch can be ignored. Also, at low frequencies impedance of C_1 is higher than R_2, the compensator behaves like an integrator for low frequencies with gain

$$\frac{1}{2\pi f C_1 R_1} \tag{31}$$

As we move towards higher frequencies, impedance of C_1 keeps decreasing and the impedance of the feedback branch starts to be dominated by R_2. The compensator acts like an inverter and the corner frequency for this transition is f_{z1}

$$f_{z1} = \frac{1}{2\pi C_1 R_2} \tag{32}$$

The gain of the compensator is

$$\frac{R_2}{R_1} \tag{33}$$

For much higher frequencies, impedance by C_3 keeps decreasing and starts to dominate the impedance of the feedback branch. The corner frequency is the second pole in the system f_{p1}

$$f_{p1} = \frac{1}{2\pi C_3 R_2} \tag{34}$$

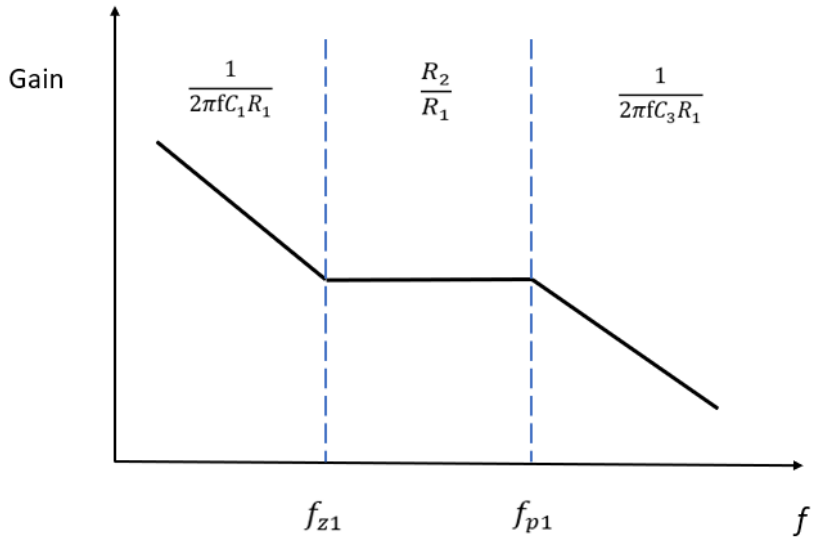


Figure 25 The frequency response of Type II analog compensator highlighting the voltage gain for the corresponding frequencies

As a conservative limit crossover frequency is allowed to go as high as 1/10th of the switching frequency.

Crossover frequency as a first approximation is f_c

$$f_c = \frac{1}{2\pi C_1 R_1} \tag{35}$$

R_1	5Ω
C_1	0.16µF
R_2	100Ω
C_3	0.005µF

Table 1 Values for passive components used to get the desired pole and zero combination

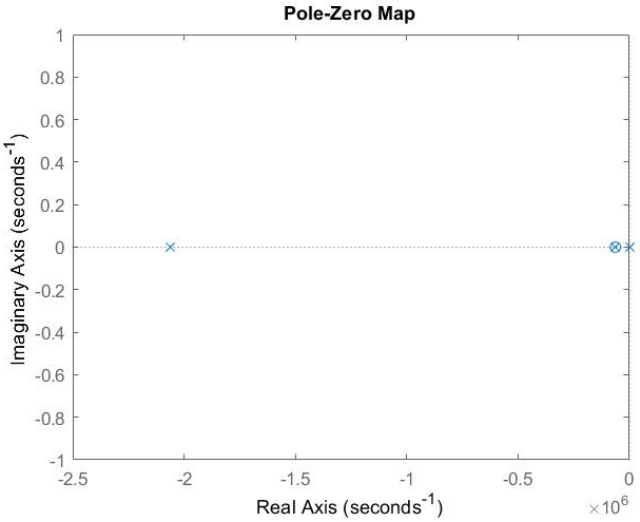


Figure 26 Pole-Zero map of closed loop transfer function (T) showing the cancellation of the plant pole by the compensator zero, a pole at DC and a pole at a frequency higher than the crossover frequency

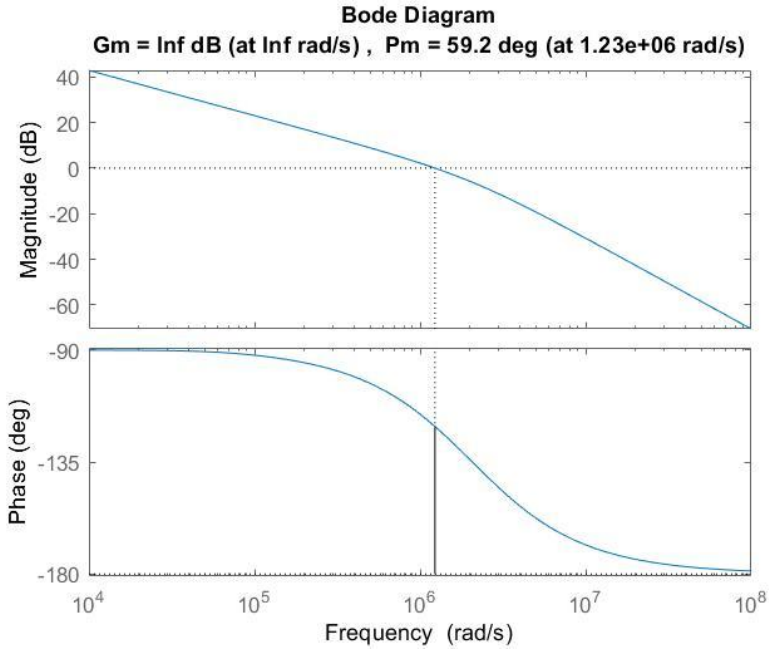


Figure 27 The frequency response of the closed loop gain (T) highlighting the phase margin (59.2˚) and the crossover frequency (195kHz)

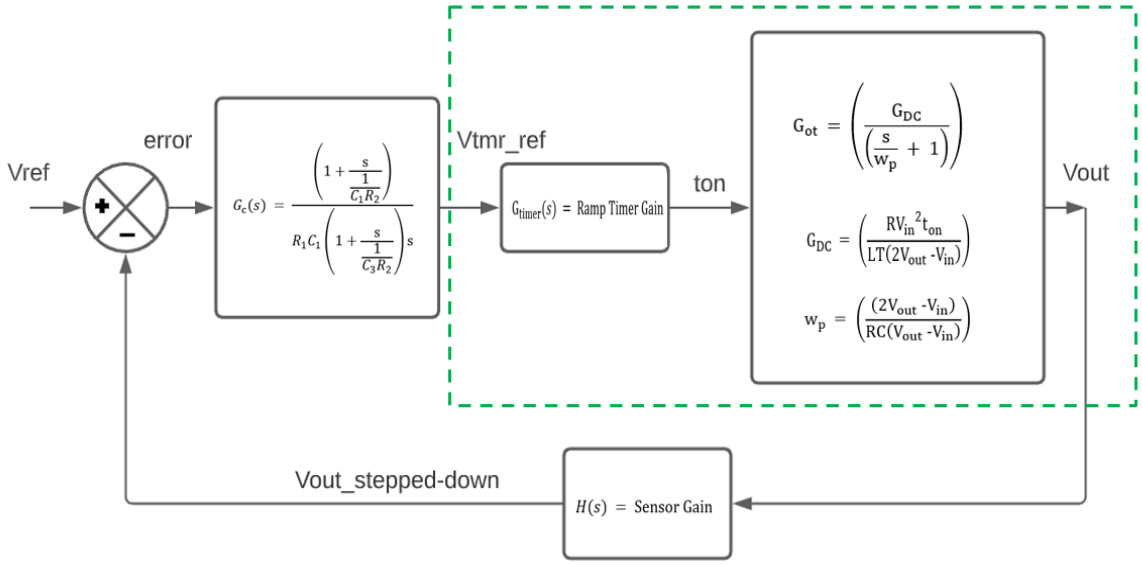


Figure 28 A block diagram highlighting the closed loop control for the converter

Following the discussed design process, a prototype 20-400V, 400W Tapped Inductor Boost converter is built. The voltage and the power ratings are chosen to target the omnipresent converter requirements. The testing procedure and the results for the same have been discussed.

Chapter 5 : Testing the Tapped Inductor and results for a 20-400V, 400W design

A 20-400V, 400W Tapped Inductor Boost converter is designed to highlight the performance. The final selected components, the testing procedure, and the tapped inductor and control test results are presented here.

DESIGN AND TESTING THE TAPPED INDUCTOR

The turns ratio for the transformer as discussed earlier is decided to be 10. Hence, the primary is consists of 10 parallel turn that are interleaved with the secondary winding as shown in Figure 29. Litz wires should be preferred over magnet wires at such high frequencies but for the prototype was build using magnet wires.

Figure 29 A sample winding structure with N parallel turns of primary interleaved with the secondary

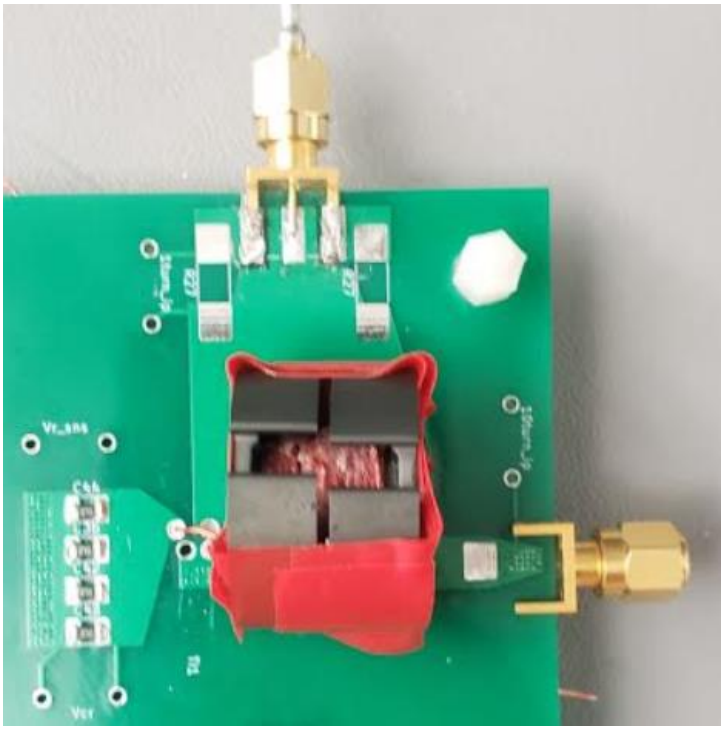


Figure 30 The testing circuit to measure the impedances of the transformer

The separate circuit to test the transformer using an impedance analyzer is shown in Figure 30. The impedances obtained are:

L_{11}	93.5nH
Impedance measured on primary when secondary shorted	8.3nH
L_{22}	11.36uH
Impedance measured on secondary when primary shorted	1.24uH

Table 2 The inductances as obtained using the testing board shown in Figure 30

Also, the voltage transformation ratio from primary to secondary is measured to be 9.42. Therefore, the inductances of the T-Model are calculated and shown in Table 3.

L_{L1}	5.5nH
L_M	88nH
L_{L2}	1.2uH

Table 3 Obtaining inductances for a T-Model from the measured inductances in Table 3

Component	Part
Core	P26/16/I-3F46
Primary and secondary wire	Turns ratio = 10, 24 AWG

Table 4 Parts used for building the Tapped Inductor

TESTING THE CONTROLS OF THE CONVERTER

Before testing the power converter, the control circuitry is tested. Hence, only the analog control circuity is soldered before any power stage components. To test the control circuit, a dummy $v_{sw,node\text{-}low}$ signal is used.. The timers and the final gating waveforms are checked to ensure the operation is as intended.

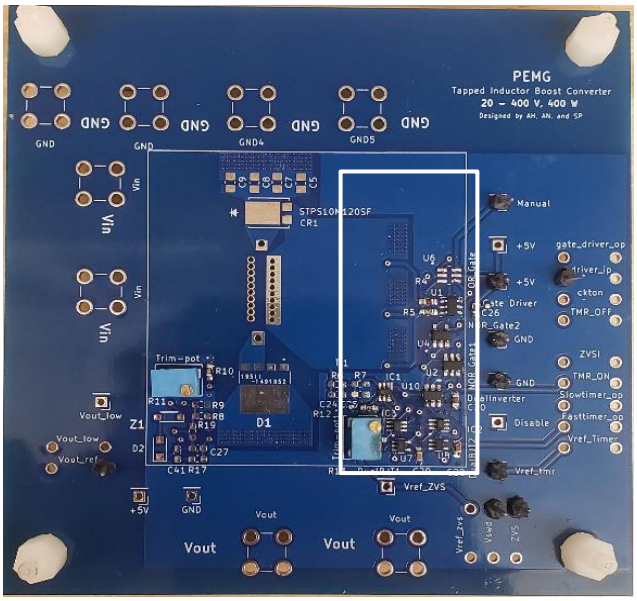


Figure 31 Control circuity added to test using a dummy $v_{sw,node\text{-}low}$ signal

Component	Part/ Value
Step-down ratio	1:20
OR Gate	SN74LVC1G332
3-input NOR Gate	SN74LVC1G27
2-input NOR Gate	SN74AHC1G02
Ramp reset FET	SN74LVC2G06
Comparator	ADCMP601
Hysteresis Resistors	150kΩ
Current mirror	2SA1873
Off timer ramp resistance	9.09kΩ
On timer ramp resistance	1kΩ
Gate Driver	LM5114
NOT Gate	SN74AHCT1G04
Op-amp	ADA4853-1AKSZ-R7
Zener Diode	MMSZ4678-TP

Table 5 Parts/values used to implement the analog control circuit

System Parameters	Value
MOSFET Q	EPC2021
$Diode_{snubber}$	STPS10M120SF
Diode	STPSC10H065DLF

Table 6 Parts/Values for the implementation of power stage

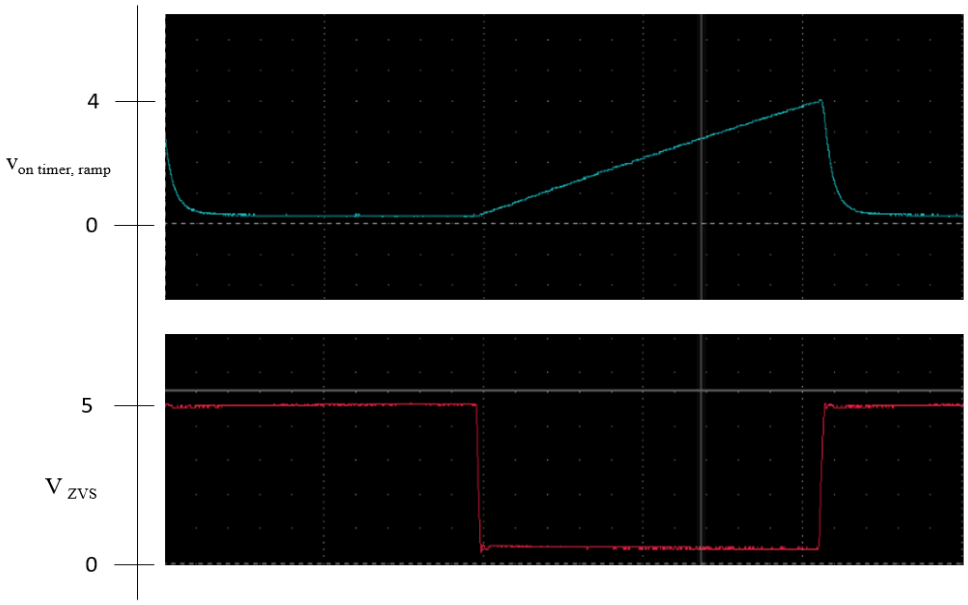


Figure 32 The V_{zvs} waveform as generated by the comparator upon being fed with dummy $V_{sw\text{-}node,low}$ (1.5MHz, 0.5 Duty PWM pulse). The V_{zvs} triggers the on-timer ramp signal as shown

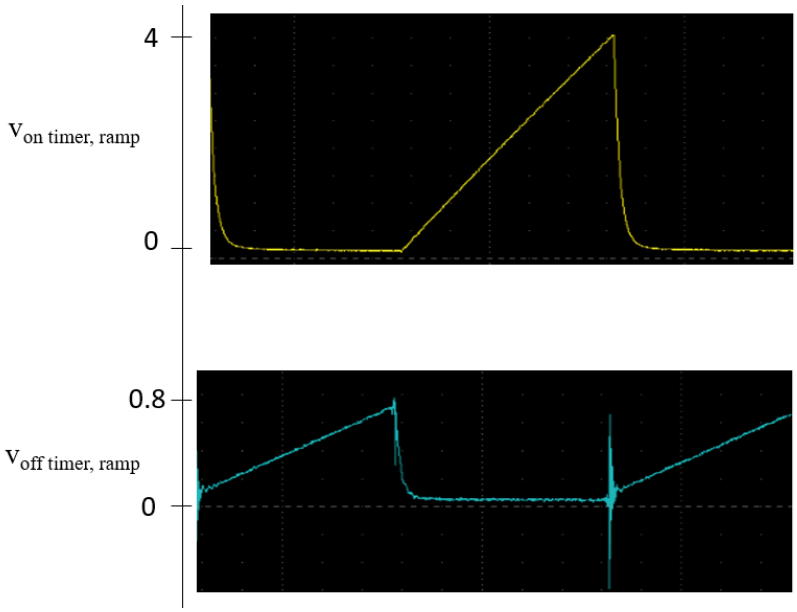


Figure 33 The V_{zvs} signal is used to create an inverter signal that helps generate an off-timer ramp as shown. The Off timer ramp is 5 timer slower than the on-timer ramp

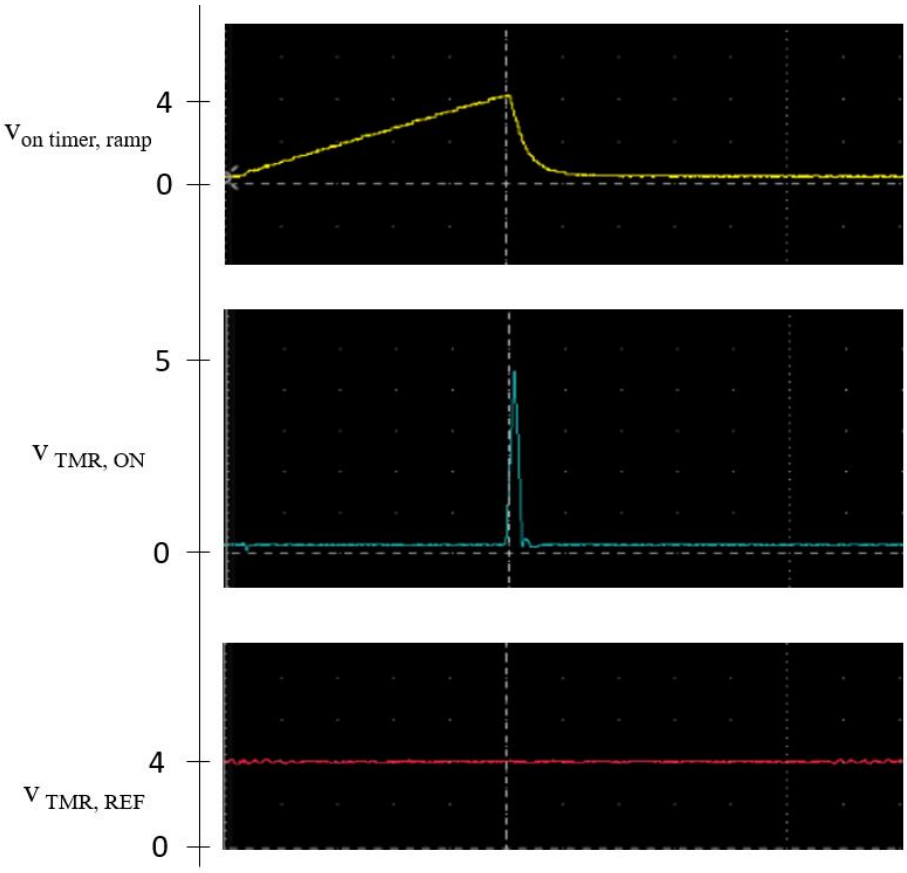


Figure 34 The on-timer ramp is compared with a $V_{TMR,REF}$ that generates a $V_{TMR,ON}$ that trigger the appropriate gating signals

POWER STAGE SIMULATION RESULTS AND INDUCTOR TESTING

The converter efficiency is very sensitive to leakage inductance. This is because of the stored energy losses due to turn-off transient as explained earlier. Using the LTSpice simulation setup, for the designed transformer, the efficiency of the converter is found to be 92%. However, adding the snubber as designed the efficiency is improved to 98.2%. Hence, a huge improvement in converter efficiency was obtained by recycling the energy stored in the leakage inductors to the load.

Also, the converter is used as a test bench to characterize the inductor. The inductances as measured using the ringing on the switch node voltage was validated with that obtained using the inductor testing circuit. The testing circuit is shown in Figure 36. The ringing to characterize the leakage can be seen in Figure 35.

The frequency of ringing oscillations is 52.1MHz. C_{oss} is assumed to be half of the maximum capacitance (=1100pF). Hence, the primary leakage inductance is 8.48nH. This is not much different as characterized by the testing circuit used as shown in Figure 30.

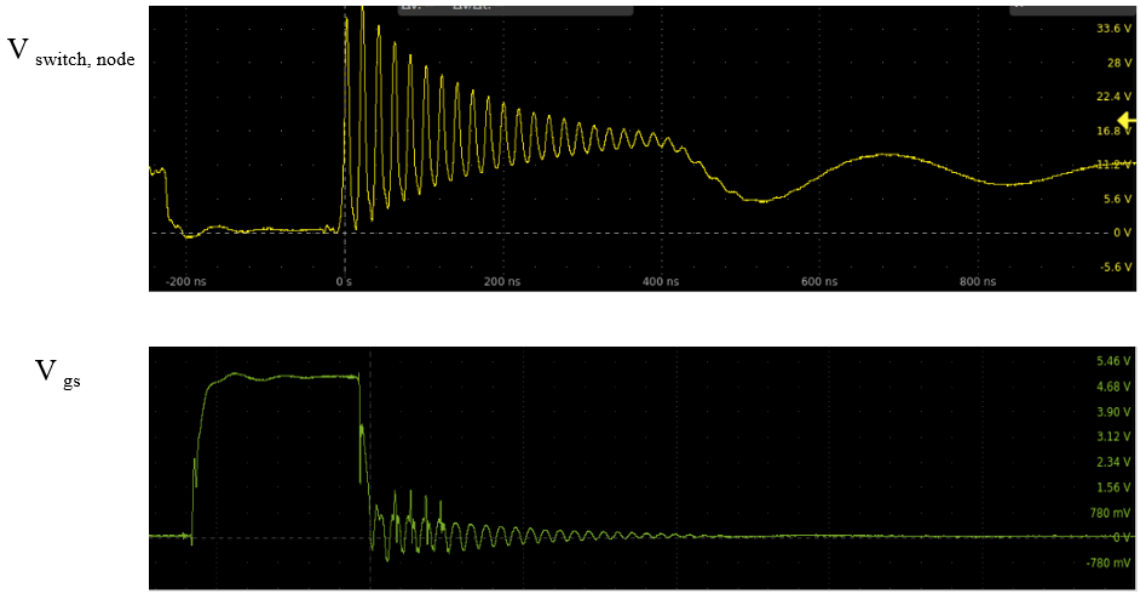


Figure 35 Switch node ringing waveform that's used to characterize the leakage of the tapped inductor

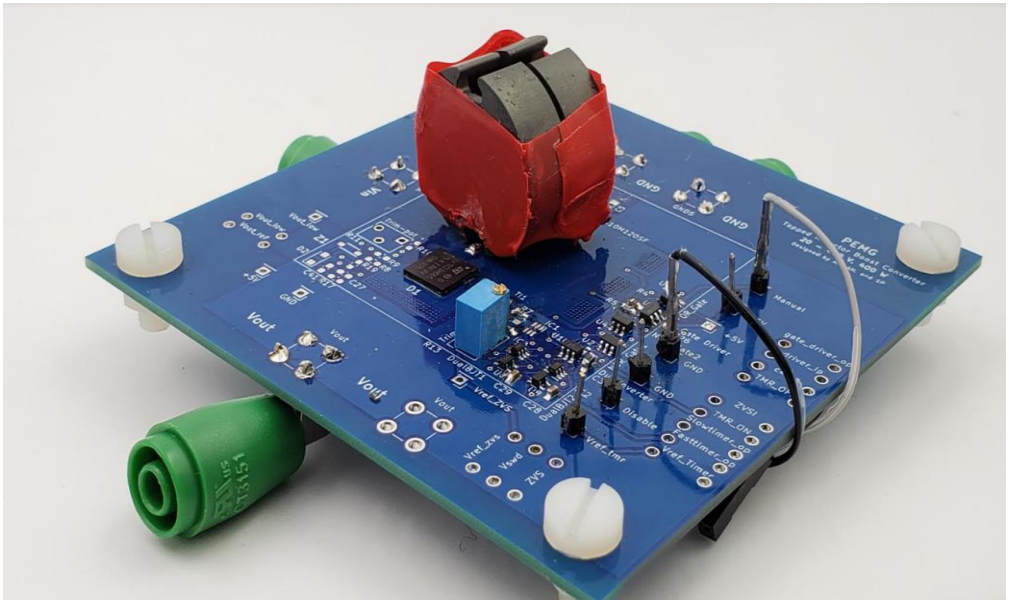


Figure 36 The testing setup used to test the built tapped inductor

POWER STAGE OPEN LOOP SIMULATION

The converter was operated in open loop (fixed $V_{TMR,REF.}$), the analog control was implemented that generated the appropriate gate pulses to obtain a valley switched turn-on to minimum stored energy turn-on switching loss. This can be seen in Figure 37. This also confirms that the off timer works as no external pulses are required to turn the converter on.

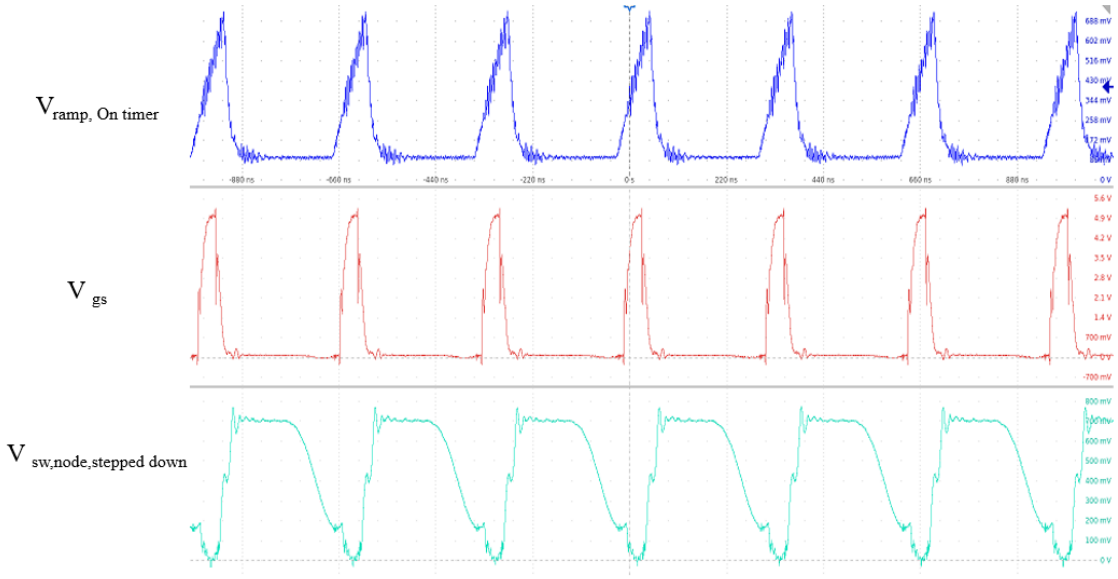


Figure 37 Top waveform showing the on timer ramp resetting after a fixed time duration given by $V_{TMR,REF.}$ This is the time period when the switch is ON. The switching node waveform indicates that the switch is turned-on when the voltage is at minimum. These waveforms are at very low load at for 10V input and 80V output

The converter was also operated in open loop (with snubber) to obtain efficiency for a 100W load. The results are shown in Table 7.

System Parameters	Value
V_{in}	10V
V_{out}	150V
P_{out}	100W
P_{in}	108.9W
Converter efficiency	91.8%

Table 7 The converter efficiency for a 100W load

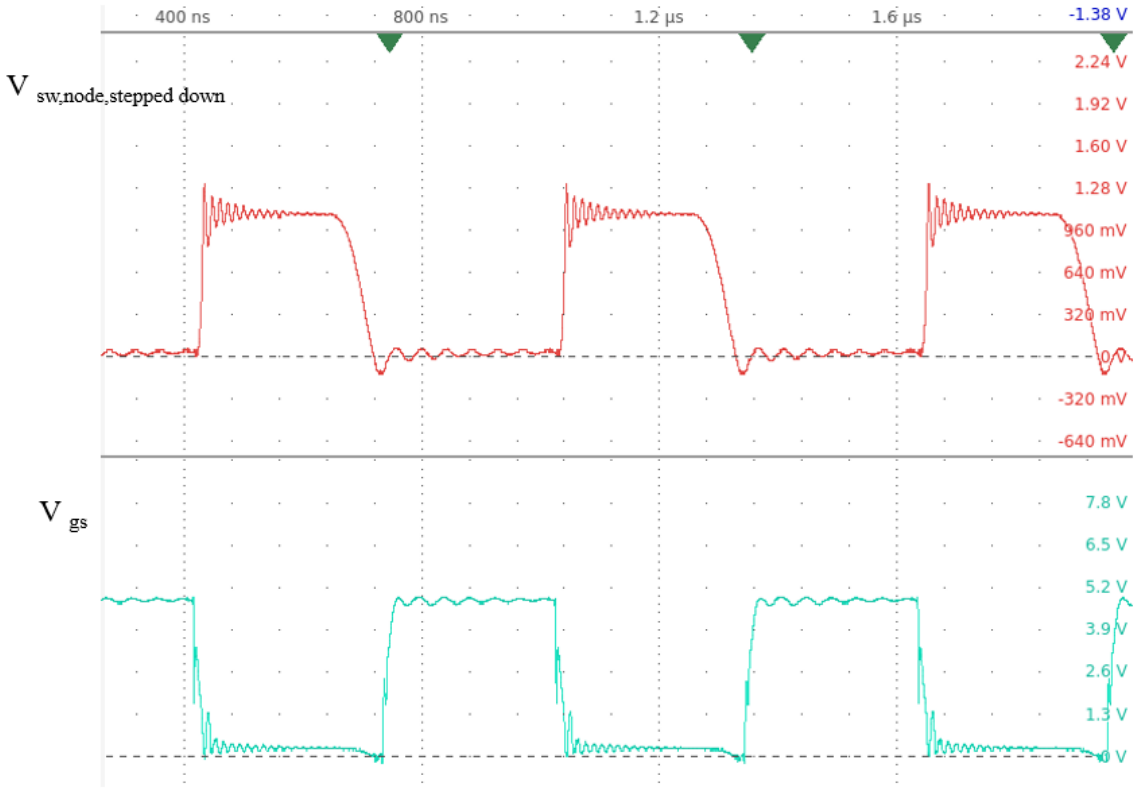


Figure 38 The stepped down switch node voltage and the gating pulse for a 10V to 150V step up and 100W output. The converter is operating at 1.6MHz, with a ZVS turn on as seen from the switching node waveform

Conclusion

This thesis explores the fact that a Tapped Inductor Boost converter can be a possible solution for a high voltage gain requirement. The topology is simple, reliable and can be designed to have an on par performance. A multi-MHz frequency operation for the converter is proposed to maximize the potential of this topology. Multi-MHz frequency helps achieve a high power density, a simple and a fast control. Operating at higher frequencies has some challenges that include stored energy losses in output parasitic capacitances of the switch and parasitic inductances (mainly leakage of the tapped inductor). These losses scale directly with frequency. To eliminate turn-on loss due to stored energy loss in C_{oss}, ZVS turn-on using valley switching operation is proposed. The design of the dedicated analog control module required to achieve a ZVS turn-on is presented. Using interleaving help minimize leakage inductance in tapped inductor and using vertical loops help minimize layout loop inductances. Additionally, the design of a loss-less passive snubber is discussed to ensure that the converter performance is not hampered due to unavoidable parasitic inductances.

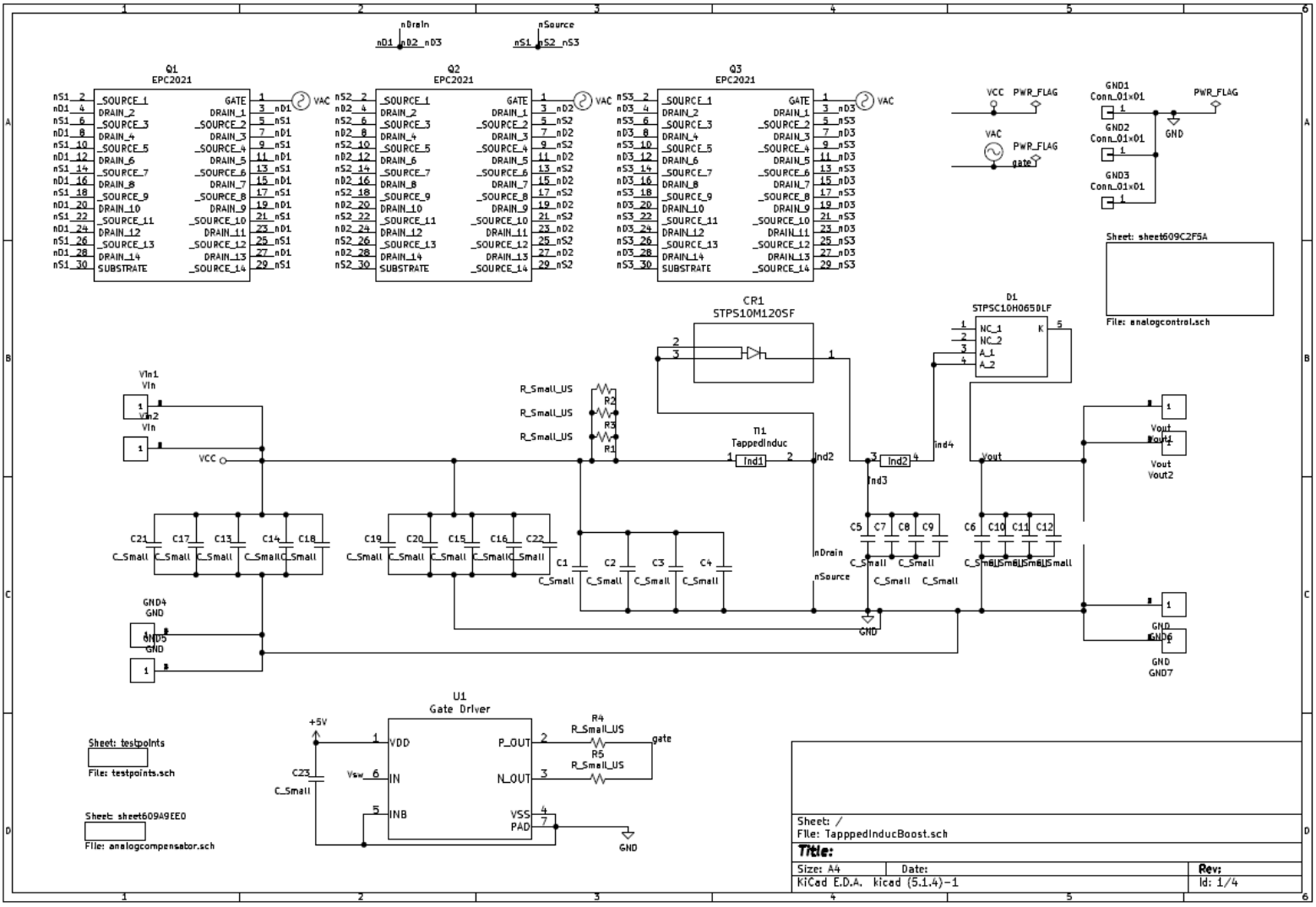
The converter also acts like a testing board to characterize the leakage of a transformer. The performance of the converter for light load is tested in open loop, the obtained efficiency is 91.8%.

FUTURE WORK

Testing the performance of the converter for full load and also to test the performance of the converter using a very low leakage (1%) tapped-inductor that's build separately.

Appendix A : Converter PCB Schematics

The schematic used to implement the prototype of the converter are shown on the following pages.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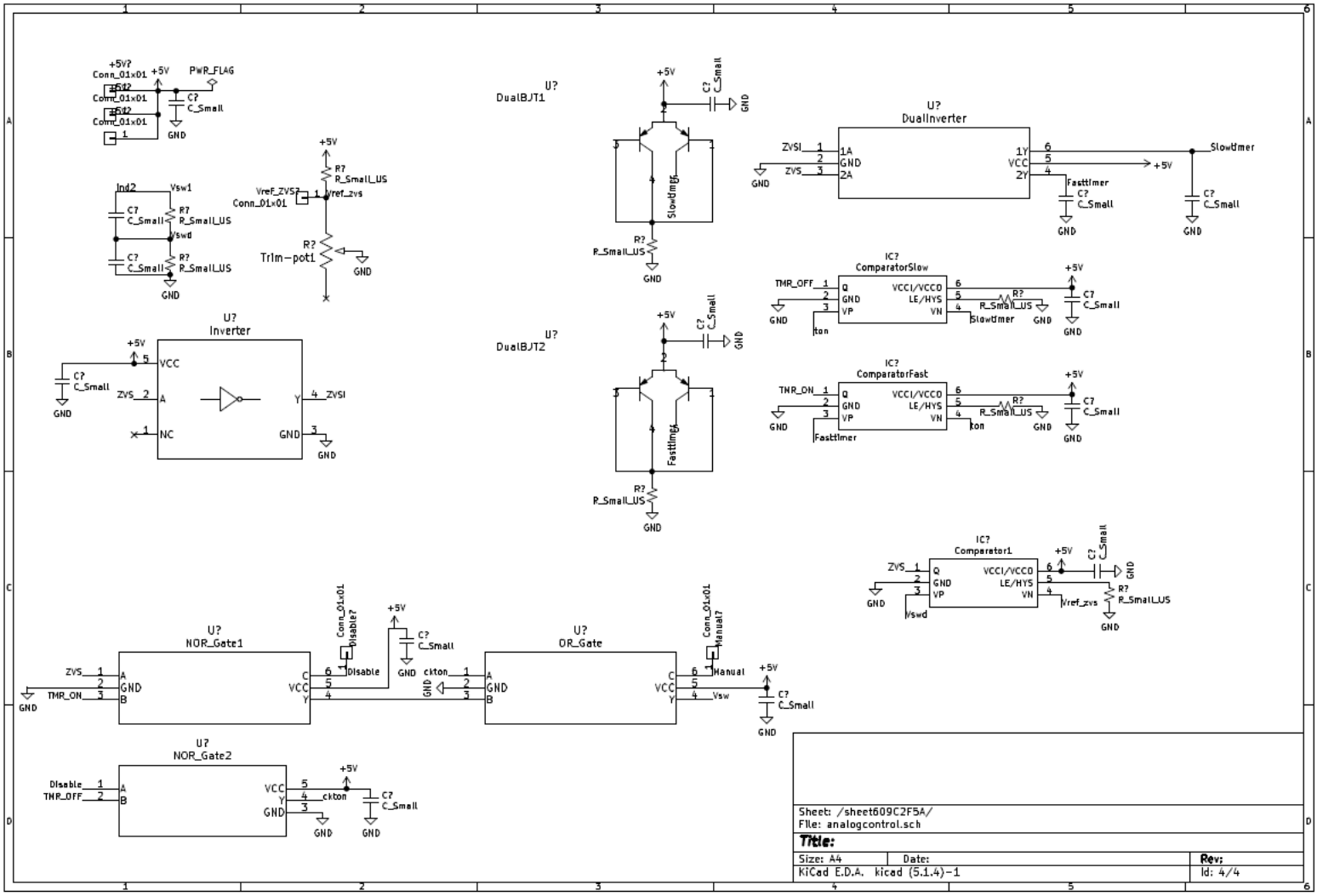
nSource
Q1
EPC2021
Q2
EPC2021
Q3
EPC2021
VAC
VCC
PWR_FLAG
GND1
Conn_01x01
GND2
Conn_01x01
GND3
Conn_01x01
GND
Sheet: sheet609C2F5A
File: analogcontrol.sch
CR1
STPS10M120SF
D1
STPSC10H065DLF
T1
TappedInduc
R_Small_US
R1
R2
R3
Vin1
Vin2
Vin
VCC
Ind1
Ind2
Ind3
Ind4
Vout
Vout1
Vout2
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C15
C16
C17
C18
C19
C20
C21
C22
C_Small
GND4
GND5
GND6
GND7
U1
Gate Driver
+5V
VDD
IN
INB
P_OUT
N_OUT
VSS
PAD
R4
R5
gate
C23
Vsw
Sheet: testpoints
File: testpoints.sch
Sheet: sheet609A9EE0
File: analogcompensator.sch
Sheet: /
File: TapppedInducBoost.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.4)-1
Id: 1/4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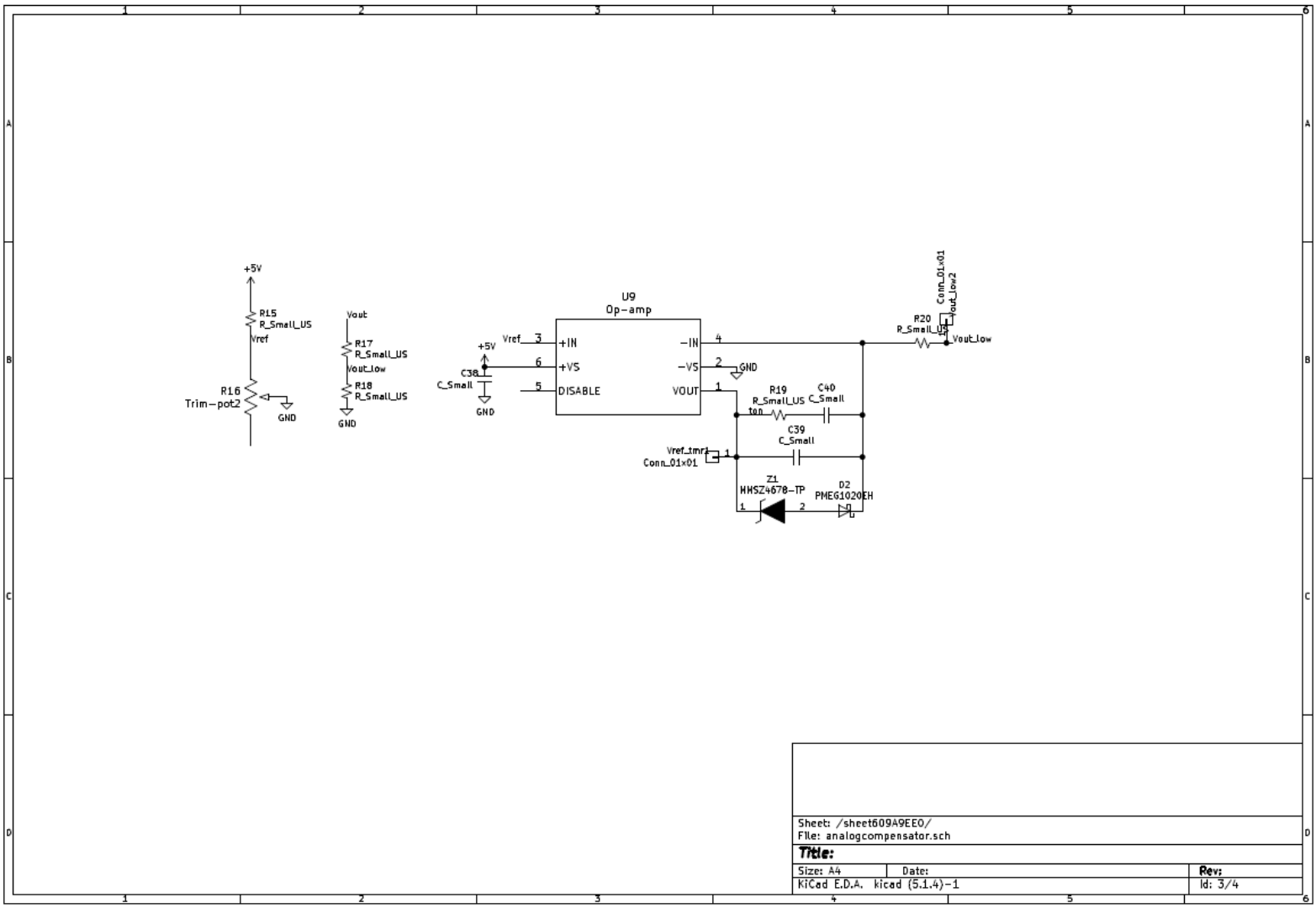
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.4)-1
Id: 4/4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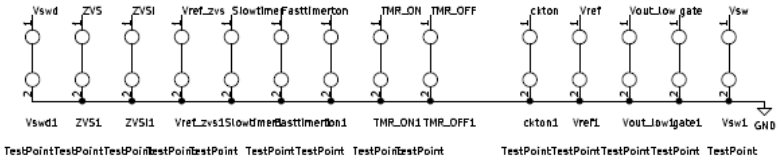
R15
R_Small_US
Vref
R16
Trim-pot2
GND
Vout
R17
R_Small_US
Vout_low
R18
R_Small_US
GND
U9
Op-amp
Vref
3
+IN
6
+VS
5
DISABLE
-IN
4
-VS
2
GND
VOUT
1
+5V
C38
C_Small
GND
R19
R_Small_US
C40
C_Small
C39
C_Small
Vref_tmr1
Conn_01x01
1
Z1
WMSZ4678-TP
1
2
D2
PMEG1020EH
R20
R_Small_US
Conn_01x01
Vout_low2
Vout_low
Sheet: /sheet609A9EE0/
File: analogcompensator.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.4)-1
Id: 3/4



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File: testpoints.sch

Title:

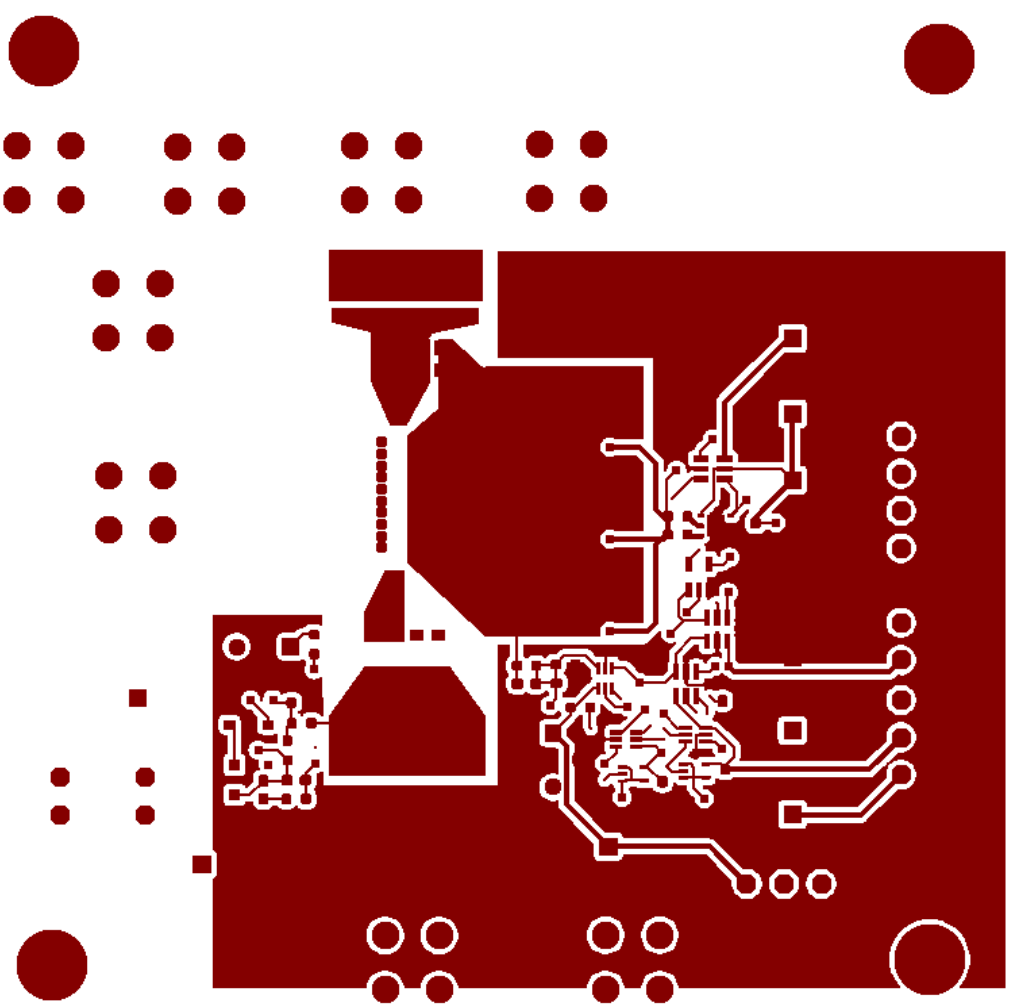
Size: A4 | Date: | Rev:

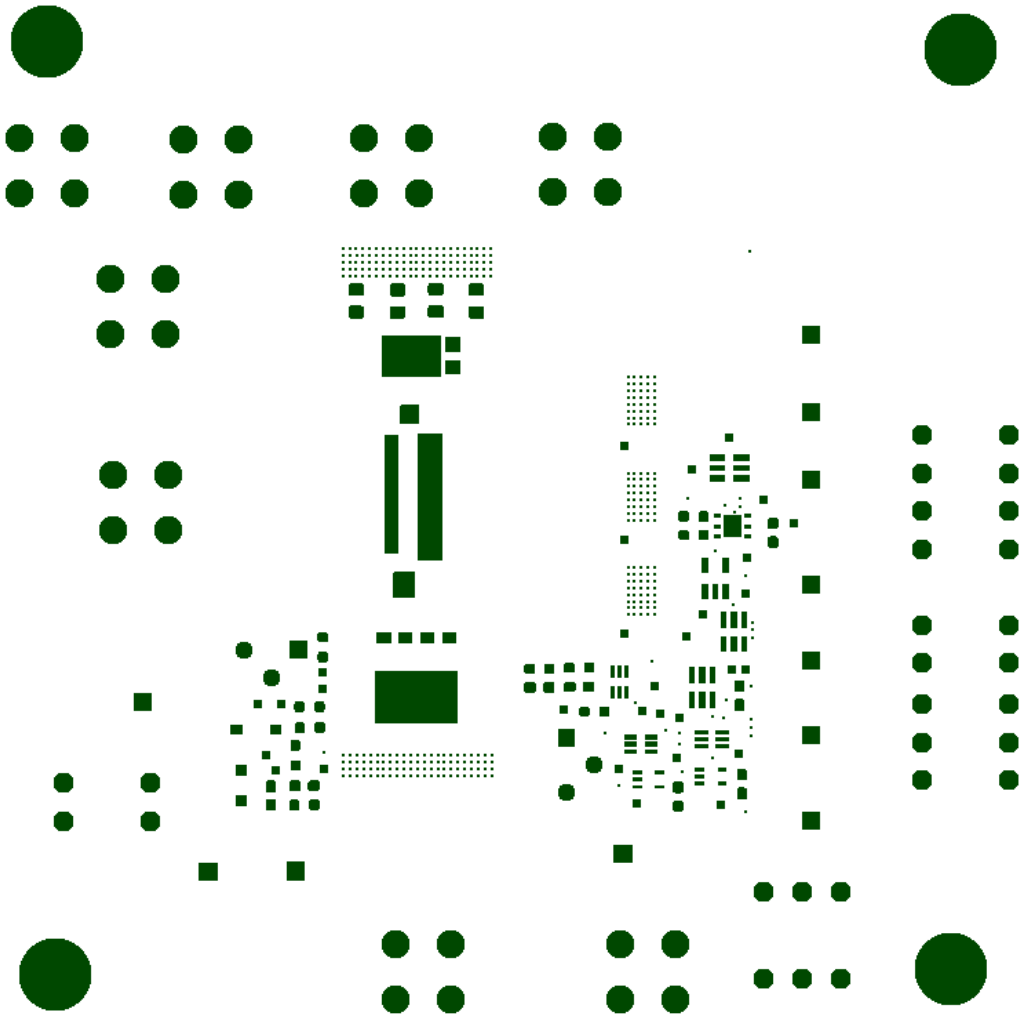
KiCad E.D.A. kicad (5.1.4)-1 | Id: 2/4

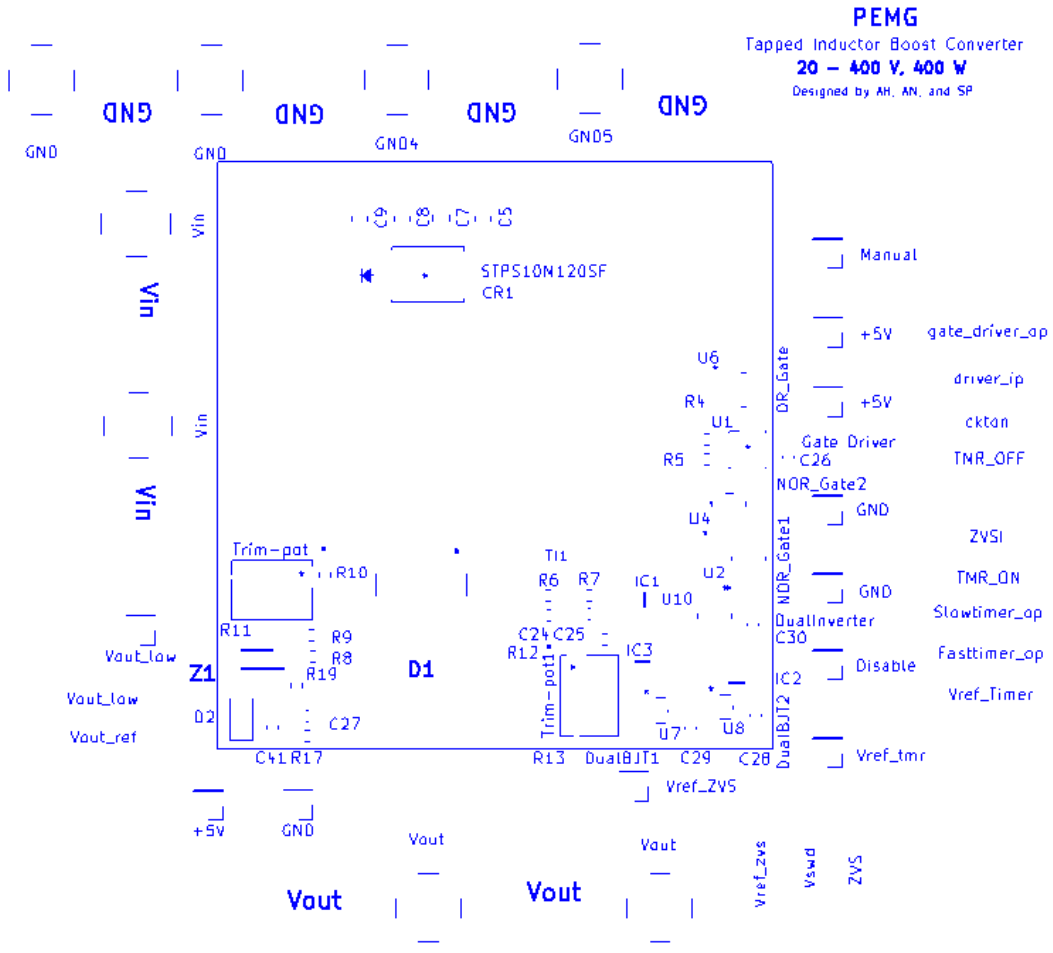
Appendix B : PCB Layout Reference

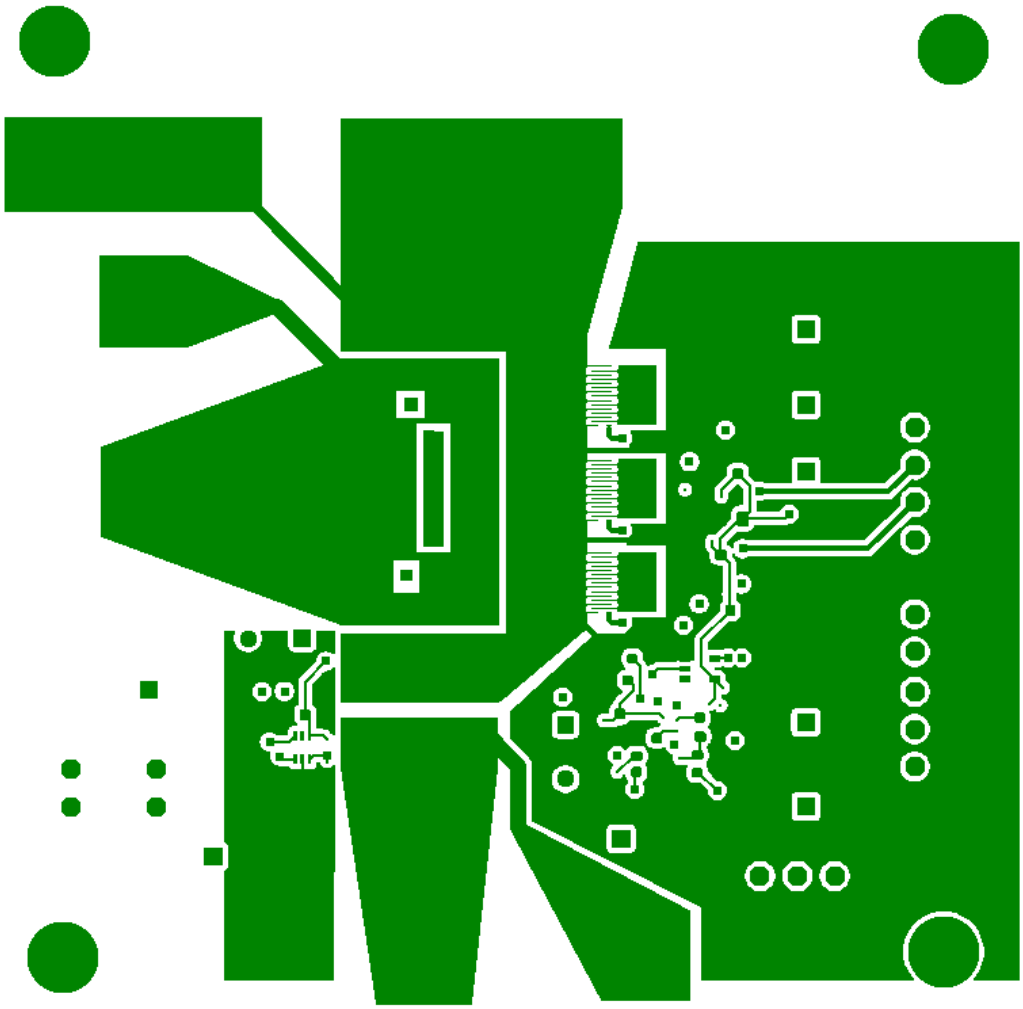
The following pages consists of the PCB layout (2.2x) of the prototype converter that was built. The files are in the following order:

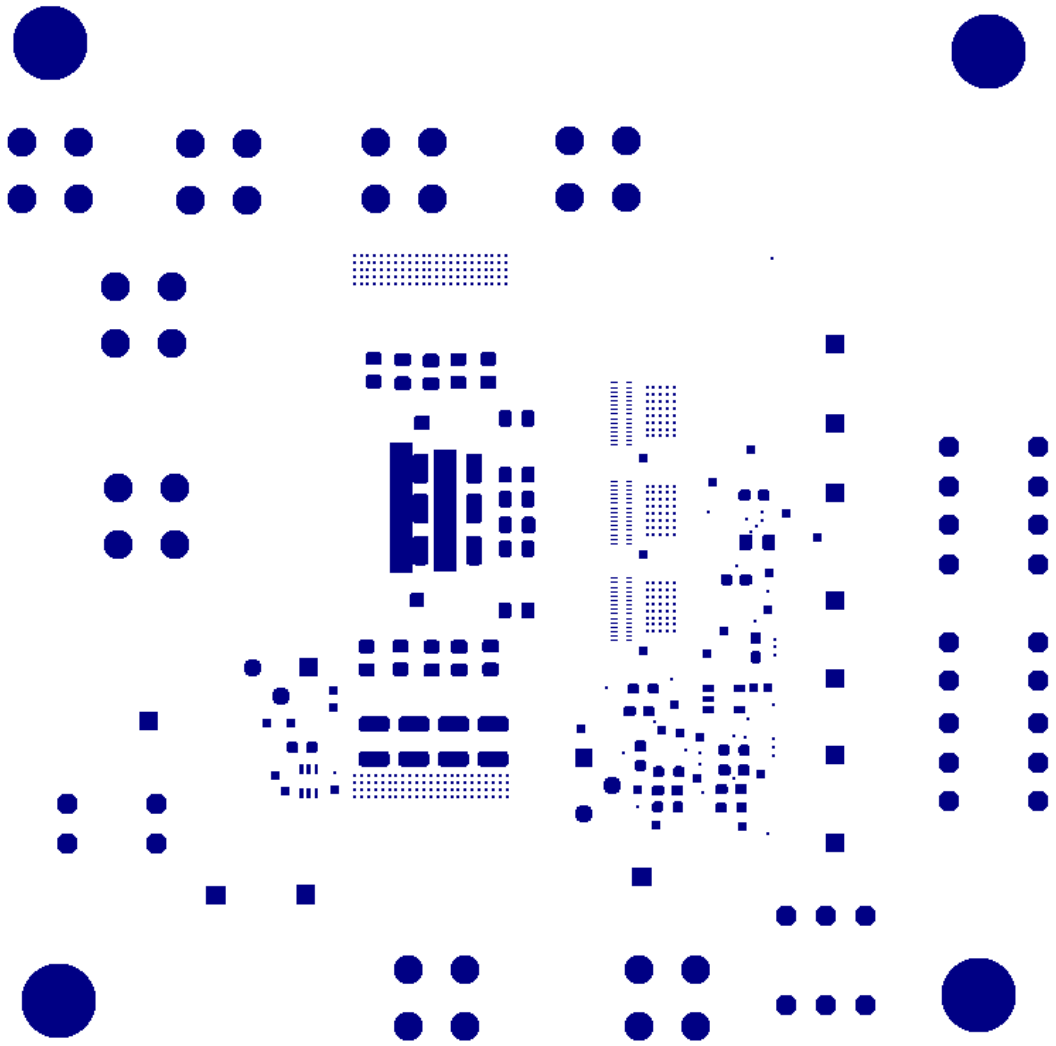
1. Top Copper
2. Top Solder Mask
3. Top Silkscreen
4. Bottom Copper
5. Bottom Solder Mask
6. Bottom Silkscreen
7. Layer 2 Copper
8. Layer 3 Copper
9. Drill



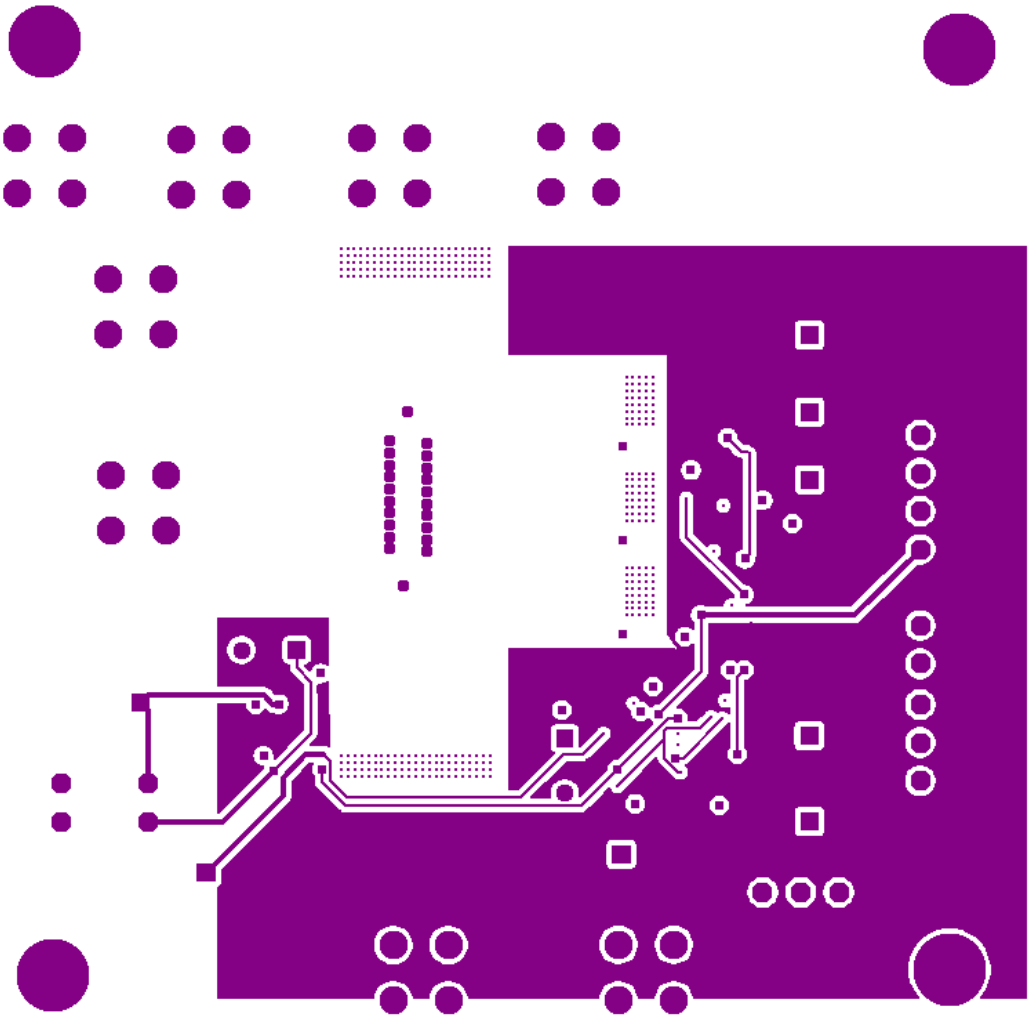


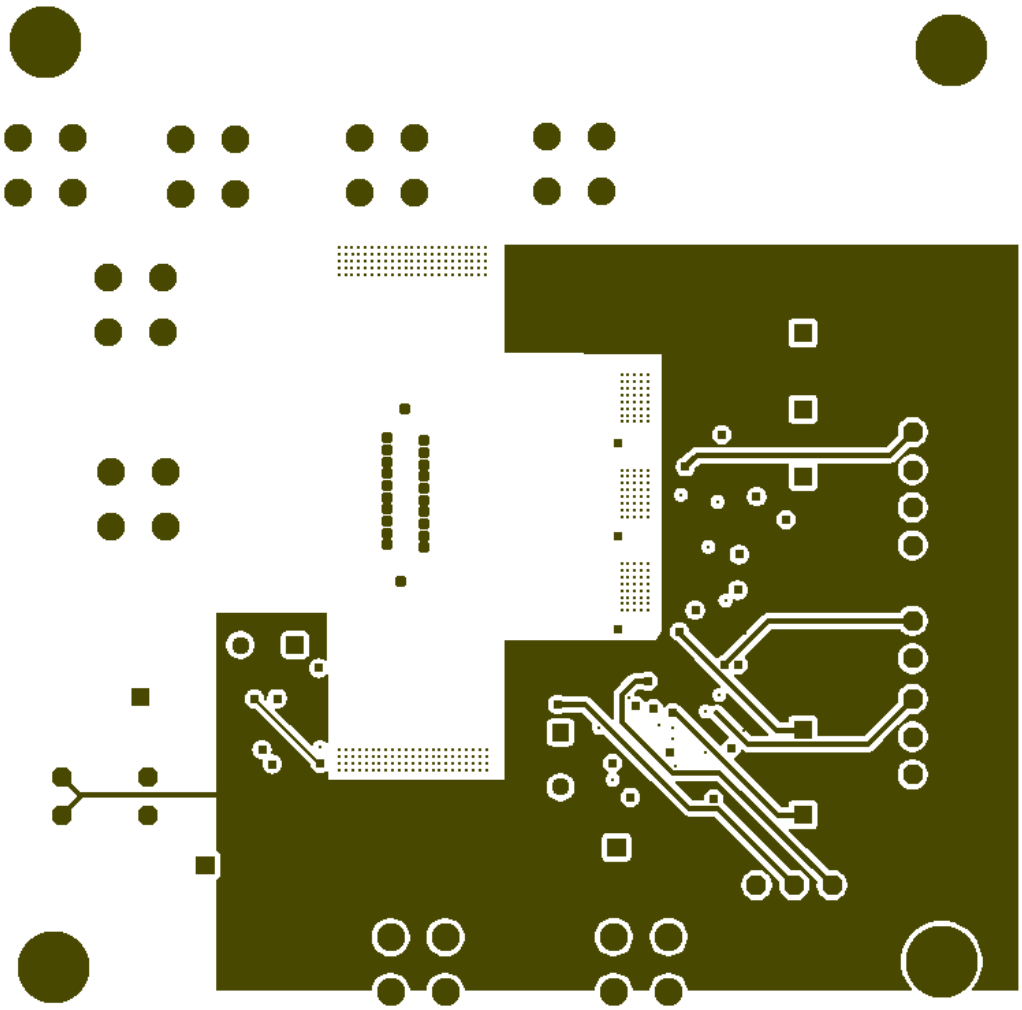

PEMG
Tapped Inductor Boost Converter
20 – 400 V, 400 W
Designed by AH, AN, and SP
GND
GND
GND
GND
GND
GND
GND4
GND5
Vin
Vin
Vin
C9
C8
C7
C5
STPS10N120SF
CR1
Manual
+5V
+5V
gate_driver_op
driver_ip
ckton
TMR_OFF
ZVSI
TMR_ON
Slowtimer_op
Fasttimer_op
Vref_Timer
Vref_tmr
DR_Gate
Gate Driver
C26
NOR_Gate2
GND
NOR_Gate1
GND
DualInverter
C30
Disable
IC2
DualBJT2
U6
R4
U1
R5
U4
U2
U10
IC1
IC3
U7
U8
C29
C28
Trim-pot
R10
R11
R9
R8
R19
C27
C41
R17
Z1
D2
D1
Vout_low
Vout_low
Vout_ref
Trim-pot1
R6
R7
C24
C25
R12
R13
DualBJT1
Vref_ZVS
+5V
GND
Vout
Vout
Vout
Vout
Vref_zvs
Vswd
ZVS

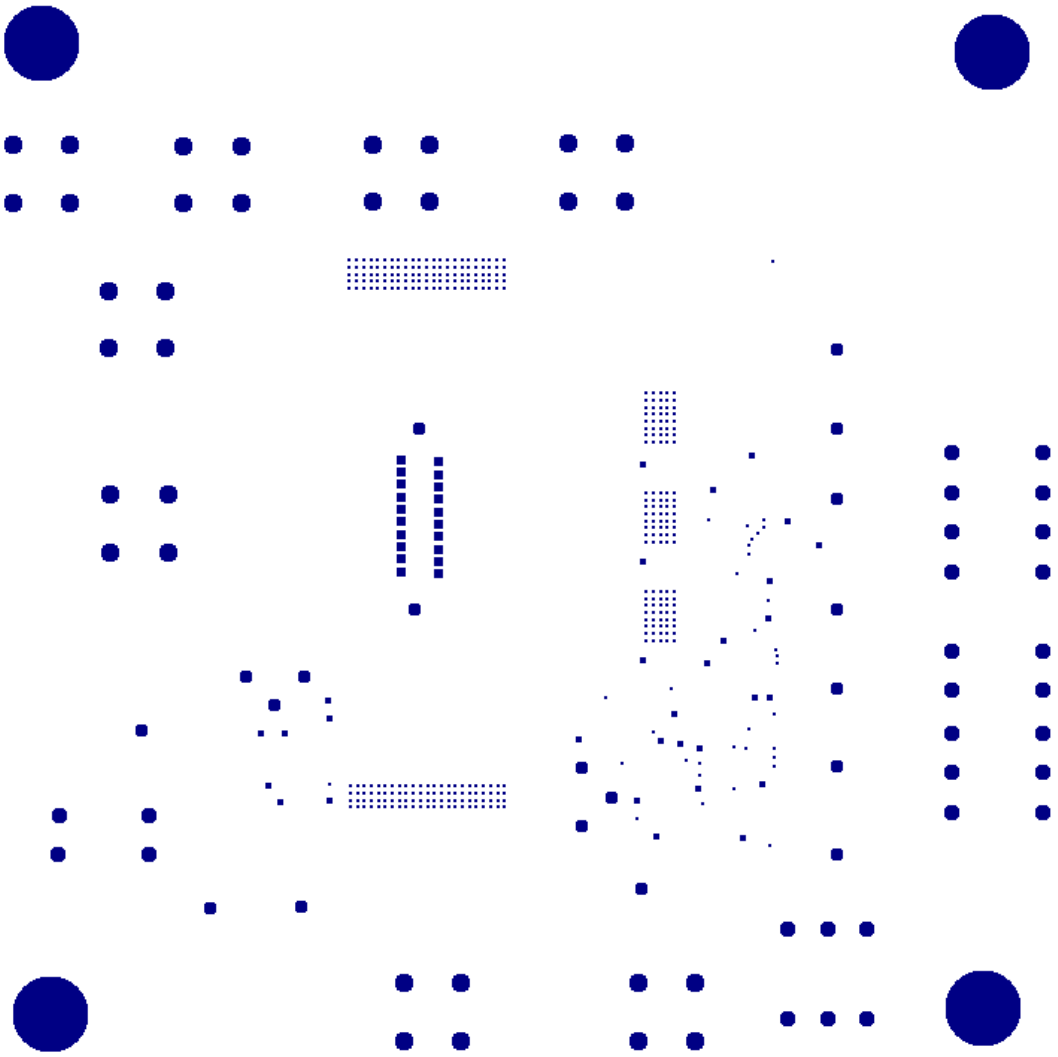




C30
C29
C28
C22
C27
C26
C25
C24
C23
C21
C20
C19
C18
C17
C16
C15
C14
C13
C12
C11
C10
C9
C8
C7
C6
C5
C4
C3
C2
C1
R1
R2
R3
Q3
Q2
Q1
C38
C39
C40
C31
R14
C34
R21
R20
U3
Inverter
C33
R16
C32
R15
C35
C37
U5
Op-amp







Appendix C : LTSpice Simulation File

The following pages consists of the .asc file that can be used to replicate the simulation of the prototype of the converter.

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WIRE -640 -768 -640 -832
WIRE 2224 -752 2224 -768
WIRE 2512 -736 2464 -736
WIRE 2656 -736 2592 -736
WIRE 2224 -720 2224 -752
WIRE 2464 -672 2464 -736
WIRE -640 -608 -640 -688
WIRE -640 -608 -800 -608
WIRE -528 -608 -640 -608
WIRE 2224 -592 2224 -640
WIRE 2848 -592 2848 -672
WIRE 2368 -528 2272 -528
WIRE 2464 -528 2464 -608
WIRE 2464 -528 2448 -528
WIRE 2512 -528 2464 -528
WIRE -800 -512 -800 -608
WIRE -528 -512 -528 -608
WIRE 2656 -512 2656 -736
WIRE 2656 -512 2576 -512
WIRE 2704 -512 2656 -512
WIRE 2512 -496 2480 -496
WIRE -672 -464 -736 -464
WIRE -592 -464 -672 -464
WIRE 2368 -432 2272 -432
WIRE 2464 -432 2448 -432
WIRE 2480 -432 2480 -496
WIRE 2480 -432 2464 -432
WIRE -672 -416 -672 -464
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WIRE -1168 -384 -1456 -384
WIRE -528 -304 -528 -416
WIRE -448 -304 -528 -304
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WIRE -528 -272 -528 -304
WIRE 2784 -272 2784 -352
WIRE -384 -256 -384 -304
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WIRE -1456 -208 -1456 -384
WIRE -1200 -208 -1360 -208
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WIRE -992 -192 -1024 -192
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WIRE -1200 -176 -1248 -176
WIRE 2240 -160 2240 -240
WIRE -3040 -144 -3040 -208
WIRE -1360 -144 -1360 -208
WIRE -800 -112 -800 -336
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WIRE -448 208 -608 208
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WIRE -736 272 -736 240
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WIRE -2784 320 -2848 320
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WIRE -2784 368 -2784 320
WIRE -1808 368 -1808 320
WIRE -864 432 -912 432
WIRE 1616 432 1616 368
WIRE -2400 464 -2416 464
WIRE -672 480 -672 448
WIRE -672 480 -800 480
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WIRE -2928 512 -3200 512
WIRE -2928 528 -2928 512
WIRE -2016 544 -2032 544
WIRE -1888 544 -1952 544
WIRE -2448 576 -2464 576
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WIRE -1888 640 -1888 624
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WIRE -2400 672 -2400 592
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WIRE -2400 800 -2608 800
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WIRE -2304 800 -2400 800
WIRE -2288 800 -2304 800
WIRE -2192 800 -2192 784
WIRE -2192 800 -2288 800
WIRE -1888 800 -1888 704
WIRE -1888 800 -2192 800
WIRE -1808 800 -1808 720
WIRE -1808 800 -1888 800
WIRE -576 848 -640 848
WIRE -464 848 -512 848
WIRE 320 864 320 704
WIRE 32 880 32 704
WIRE 208 880 176 880
WIRE 288 880 208 880
WIRE 496 896 352 896
WIRE 288 912 112 912
WIRE 1728 928 1728 592
WIRE 32 1024 32 960
WIRE 256 1024 32 1024
WIRE 320 1024 320 928
WIRE 320 1024 256 1024
WIRE -1152 1056 -1440 1056
WIRE 1728 1056 1728 1008
WIRE 1888 1056 1728 1056
WIRE 256 1104 256 1024
WIRE 1728 1104 1728 1056
WIRE -1152 1216 -1152 1056
WIRE -1440 1232 -1440 1056
WIRE -1344 1232 -1360 1232
WIRE -1184 1232 -1344 1232
WIRE 1728 1232 1728 1184
WIRE -976 1248 -1120 1248
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```
WIRE -1216 1264 -1280 1264
WIRE -1184 1264 -1216 1264
WIRE -1440 1376 -1440 1312
WIRE -1216 1376 -1440 1376
WIRE -1152 1376 -1152 1280
WIRE -1152 1376 -1216 1376
WIRE -1216 1456 -1216 1376
FLAG -2256 224 Vsw
FLAG -2256 304 0
FLAG -2448 768 Vswfinal
FLAG -2448 720 0
FLAG -2288 800 0
FLAG -1840 624 Vout
FLAG -2400 464 Vsw1
FLAG -1216 1264 Fasttimer
FLAG -1216 1456 0
FLAG -976 1248 TMRON
FLAG -1232 16 0
FLAG -1808 368 0
FLAG -1808 96 Vsw1
FLAG -1808 208 Vswd
FLAG -1248 -176 Vswd
FLAG -1024 -192 ZVS
FLAG -1056 144 ZVS
FLAG -1056 272 TMRON
FLAG -1040 208 Disable
FLAG -448 208 Vswlow
FLAG -752 336 Vsw
FLAG 608 576 Disable
FLAG 608 656 0
FLAG 1616 368 0
FLAG 1680 944 0
FLAG 1680 992 Vswlow
FLAG 1888 1056 Vswfinal
FLAG 1728 1232 0
FLAG 208 880 Slowtimer
FLAG 256 1104 0
FLAG 496 896 TMROFF
FLAG 240 208 Disable
FLAG 304 208 Enable
FLAG -928 496 TMROFF
FLAG -672 448 ckton
```

```
FLAG -784 272 ckton
FLAG -912 432 Disable
FLAG 2848 -592 0
FLAG 2784 -432 0
FLAG 2848 -752 Vcc+
FLAG 2784 -272 Vcc-
FLAG 2240 -160 0
FLAG 2240 -320 Vref
FLAG 2272 -528 Vout_low
FLAG 2272 -432 Vref
FLAG 2464 -352 0
FLAG 2544 -544 Vcc+
FLAG 2544 -480 Vcc-
FLAG 2224 -880 Vout
FLAG 2224 -592 0
FLAG 2224 -752 Vout_low
FLAG 2704 -512 ton
FLAG -1344 1232 ton
FLAG 112 912 ton
FLAG -2976 416 ZVS
FLAG -2928 528 0
FLAG -3040 -208 0
FLAG -2784 432 0
FLAG -2976 368 0
FLAG -2848 320 Fasttimer
FLAG -576 -208 ZVSI
FLAG -528 -96 0
FLAG -640 -832 0
FLAG -384 -192 0
FLAG -576 -256 0
FLAG -448 -304 Slowtimer
FLAG -640 848 ZVS
FLAG -464 848 ZVSI
SYMBOL voltage -2256 208 R0
WINDOW 3 -264 -440 Left 2
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR Value PULSE(0 10 0 1n 1n 495n 800n 1)
SYMATTR InstName V1
SYMBOL ind2 -2512 608 R270
WINDOW 0 32 56 VTop 2
WINDOW 3 -27 57 VTop 2
```

```
SYMATTR InstName L1
SYMATTR Value 1.3m
SYMATTR Type ind
SYMATTR SpiceLine Rser=1m
SYMBOL cap -1904 640 R0
SYMATTR InstName C1
SYMATTR Value 10µ
SYMBOL res -1824 624 R0
SYMATTR InstName R1
SYMATTR Value 400
SYMBOL voltage -2608 640 R0
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR InstName V2
SYMATTR Value 20
SYMBOL sw -2400 688 R0
WINDOW 0 -10 165 Left 2
WINDOW 3 -33 134 Left 2
SYMATTR InstName S1
SYMATTR Value Mysw
SYMBOL ind2 -2288 592 R270
WINDOW 0 32 56 VTop 2
WINDOW 3 -26 57 VTop 2
SYMATTR InstName L2
SYMATTR Value 130m
SYMATTR Type ind
SYMBOL ind -2608 608 R270
WINDOW 0 32 56 VTop 2
WINDOW 3 4 56 VBottom 2
SYMATTR InstName Ll1
SYMATTR Value 5n
SYMBOL ind -2208 592 R270
WINDOW 0 32 56 VTop 2
WINDOW 3 4 56 VBottom 2
SYMATTR InstName Ll2
SYMATTR Value 50n
SYMBOL ind -2512 480 R270
WINDOW 0 32 56 VTop 2
WINDOW 3 3 57 VBottom 2
SYMATTR InstName Lm1
SYMATTR Value 105n
SYMBOL cap -2320 704 R0
```

```
WINDOW 0 -36 32 Left 2
WINDOW 3 -43 61 Left 2
SYMATTR InstName C2
SYMATTR Value 1450p
SYMBOL diode -2176 784 R180
WINDOW 0 -23 60 Left 2
WINDOW 3 -33 -42 Left 2
SYMATTR InstName D1
SYMATTR Value mydiode
SYMBOL diode -2016 560 R270
WINDOW 0 32 32 VTop 2
WINDOW 3 -14 26 VBottom 2
SYMATTR InstName D2
SYMATTR Value mydiode
SYMBOL Comparators\\LT1720 -1152 1184 R0
SYMATTR InstName U1
SYMBOL voltage -1440 1216 R0
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR InstName V3
SYMATTR Value 5
SYMBOL Comparators\\LT1720 -1168 -256 R0
SYMATTR InstName U2
SYMBOL voltage -1456 -224 R0
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR InstName V4
SYMATTR Value 5
SYMBOL voltage -1360 -160 R0
WINDOW 0 38 56 Left 2
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR InstName V5
SYMATTR Value 0.1
SYMBOL res -1824 96 R0
SYMATTR InstName R2
SYMATTR Value 19k
SYMBOL res -1824 224 R0
SYMATTR InstName R3
SYMATTR Value 1k
SYMBOL Digital\\or -848 144 R0
SYMATTR InstName A1
```

```
SYMBOL Digital\\or -640 160 R0
SYMATTR InstName A2
SYMBOL voltage 608 560 R0
WINDOW 3 44 67 Left 2
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR Value PWL(0 1 500n 1 500.001n 0)
SYMATTR InstName V6
SYMBOL voltage 1616 528 R180
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR InstName V7
SYMATTR Value 12
SYMBOL sw 1728 912 R0
SYMATTR InstName S2
SYMATTR Value SW1
SYMBOL res 1712 1088 R0
SYMATTR InstName R4
SYMATTR Value 2k
SYMBOL Comparators\\LT1720 320 832 R0
SYMATTR InstName U3
SYMBOL voltage 32 864 R0
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR InstName V8
SYMATTR Value 5
SYMBOL Digital\\inv 240 144 R0
SYMATTR InstName A3
SYMBOL Digital\\or -832 400 R0
SYMATTR InstName A4
SYMBOL res 2464 -544 R90
WINDOW 0 7 146 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName R5
SYMATTR Value 100
SYMBOL res 2464 -448 R90
WINDOW 0 14 148 VBottom 2
WINDOW 3 39 57 VTop 2
SYMATTR InstName R6
SYMATTR Value 100
SYMBOL res 2496 -720 R270
WINDOW 0 32 56 VTop 2
```

```
WINDOW 3 0 56 VBottom 2
SYMATTR InstName R7
SYMATTR Value 100
SYMBOL voltage 2240 -336 R0
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR InstName V9
SYMATTR Value 2.6667
SYMBOL voltage 2848 -768 R0
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR InstName V10
SYMATTR Value 3.3
SYMBOL voltage 2784 -448 R0
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR InstName V11
SYMATTR Value 0
SYMBOL res 2480 -336 R180
WINDOW 0 -63 21 Left 2
WINDOW 3 -65 56 Left 2
SYMATTR InstName R8
SYMATTR Value 10000
SYMBOL Opamps\\LT1498 2544 -576 R0
SYMATTR InstName U4
SYMBOL cap 2448 -672 R0
SYMATTR InstName C4
SYMATTR Value 0.01µ
SYMBOL res 2208 -864 R0
SYMATTR InstName R9
SYMATTR Value 149k
SYMBOL res 2208 -736 R0
SYMATTR InstName R10
SYMATTR Value 1k
SYMBOL cap -2800 368 R0
SYMATTR InstName C5
SYMATTR Value 0.001µ
SYMBOL voltage -3040 -48 R180
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR InstName V12
SYMATTR Value 5
```

```
SYMBOL res -3216 192 R0
SYMATTR InstName R11
SYMATTR Value 1k
SYMBOL sw -2928 336 R0
SYMATTR InstName S3
SYMATTR Value SW1
SYMBOL pnp -2992 208 M180
SYMATTR InstName Q1
SYMATTR Value 2N2907
SYMBOL pnp -3136 208 R180
SYMATTR InstName Q2
SYMATTR Value 2N2907
SYMBOL cap -400 -256 R0
SYMATTR InstName C6
SYMATTR Value 0.001µ
SYMBOL voltage -640 -672 R180
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR InstName V13
SYMATTR Value 5
SYMBOL res -816 -432 R0
SYMATTR InstName R12
SYMATTR Value 2k
SYMBOL sw -528 -288 R0
SYMATTR InstName S4
SYMATTR Value SW1
SYMBOL pnp -592 -416 M180
SYMATTR InstName Q3
SYMATTR Value 2N2907
SYMBOL pnp -736 -416 R180
SYMATTR InstName Q4
SYMATTR Value 2N2907
SYMBOL Digital\\inv -576 784 R0
SYMATTR InstName A5
TEXT -2592 -384 Left 2 !.model Mysw SW(Ron = 0.010 Roff = 100Meg
Vt = 2.5)
TEXT -2448 -336 Left 2 !.model mydiode D(Vfwd = 0.1)
TEXT -2360 528 Left 2 !K L1 L2 1
TEXT -2600 -424 Left 2 !.model SW1 SW(Ron = 0.00001 Roff = 100Meg
Vt = 0.5)
TEXT -2320 -592 Left 2 !.tran 5m
TEXT 1584 248 Left 2 ;PulseAmplification
```

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